The Stimulus Test Stand

L. Christofek, P. Rapidis, A. Reinhard

Abstract: We provide a description of the Stimulus Test Stand used for prototype testing of the SVX4 chip.

1 Introduction

The Stimulus Test Stand was originally constructed and assembled for testing the SVX2 ASIC readout and then upgraded for SVX3 ASIC prototyping and testing. We have modified this system for SVX4 ASIC [1] prototype testing. We described the individual components below. Additional details for other hardware for SVX4 testing can be found in reference [2].

2 Overview

The Stimulus Test Stand consists of a PC with a GPIB interface card, a DAC-812 and a PCL-710 digital counter that are connected through ISA ports. A custom DAQ program called SVXEval was written for Windows 9x operating system. The SVXEval program initializes all the components in the test stand via GPIB. It is used to algorithmically construct the control patterns needed by the SVX4 and to send them to the Tektronix HFS 9003 Stimulus System. The PC is a 200 MHz Pentium with 64 MB of RAM and is running Windows 98. We show the entire system in Figure 1.

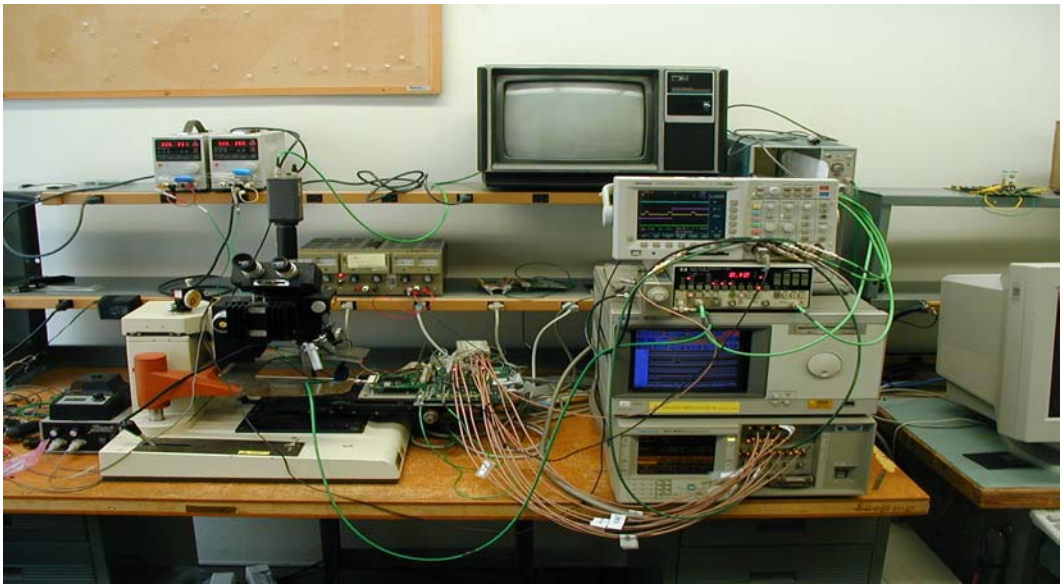

Figure 1: The Stimulus Test Stand. The PC is located to the far right. The Stimulus System is located next to the PC below the TektronixTDS 3034 Oscilloscope, the HP Pulse Generator, and Logic Analyzer (in order from top to bottom). In the middle of the picture, the cables connecting the Stimulus System outputs to the SVX4 adaptor board can be seen. An SVX4 chip carrier can be seen connected to the adaptor board. The adaptor board and chip carrier are mounted on the movable table of the Rucker & Kolls Probe Station that has a Bausch & Lomb MicroZoom microscope connected to the television. The power supplies for the adaptor board and SVX4 chip can be seen, as well as the power supply for the two Picoprobes that are used to probe the test pads located on top of the SVX4 chip itself.

In Figure 2, we show a cartoon representation of the hardware for the Stimulus Test Stand. The computer sends a pattern to the Stimulus System via the SVX4 adaptor board. The SVX4 chip is mounted onto a carrier board. The data from the chip is stored in FIFOs on the adaptor board until the computer can read out the data. The Logic

Analyzer has two pods that probe test points on the adaptor board and gives a graphical representation of the waveform and the data output of the SVX4 chip.

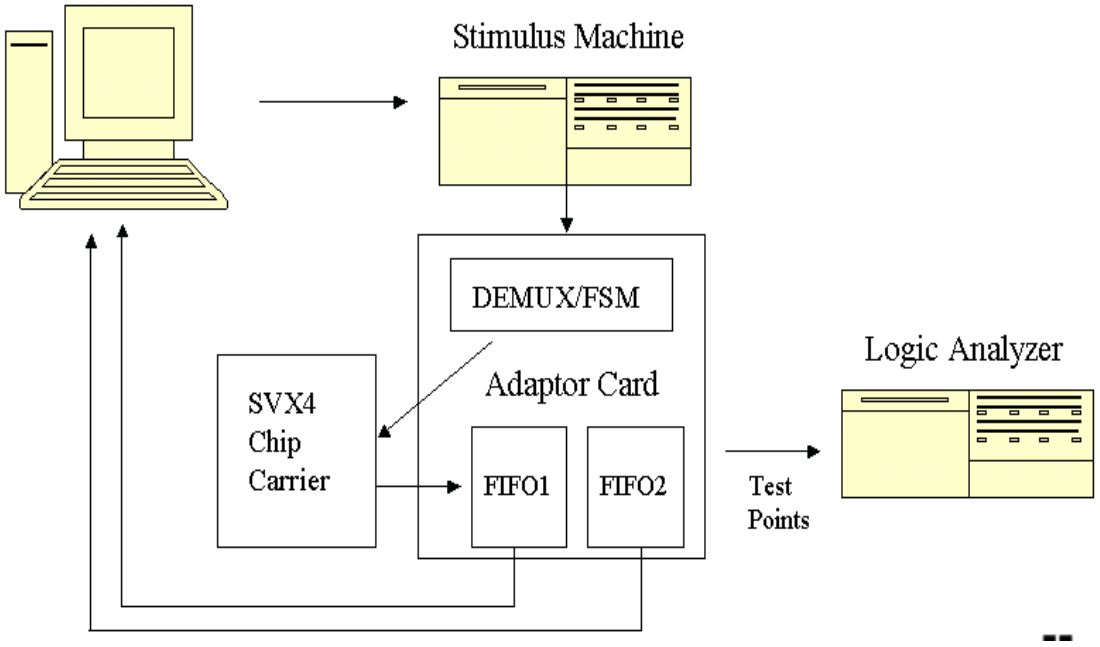

Figure 2 Cartoon representation of the Stimulus Test Stand. The PC is connected to the Stimulus System and the Logic Analyzer through a GPIB interface. The SVX4 adaptor board is shown in the middle with the demultiplexer/finite state machine (programmed inside the EPLD located on the board) that is used to generate the additional control signals for proper SVX4 operation.

2.1 The SVX4 Chip Carrier

The SVX4 chip carrier provides a platform in which to interact with the SVX4 chip. It is a small square PCB that acts as a rigidifier and heat sink for the SVX4 die. It provides various electrical pads for proper power connections and locations for passive components for internal biasing of the SVX4 and other multipin connectors. In Figure 3, we show an actual SVX4 chip carrier used in the test stand. In Figure 4, we show the schematic for the SVX4 chip carrier.

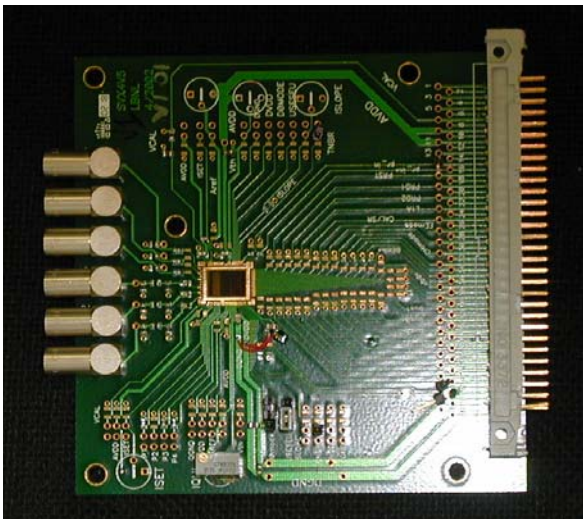

Figure 3: The SVX4 chip carrier. This chip carrier is fully stuffed and contains an SVX4 chip in the middle of the PC board. The left side of the chip carrier has mounted Lemo connectors allowing charge injection through a capacitor into individually bonded channels of the SVX4 chip. The 60-pin connector to the right is used to make an electrical connection with the SVX4 adaptor board.

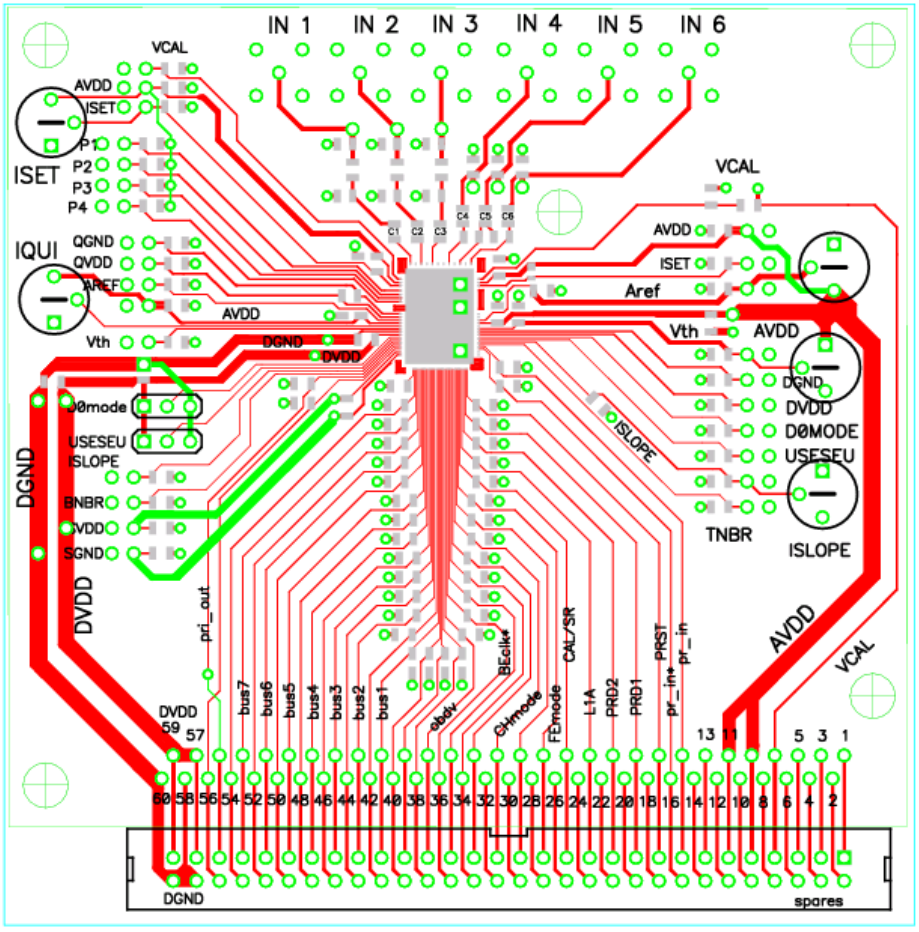

Figure 4 The schematic for the SVX4 chip carrier.

2.2 The SVX4 Adaptor Board

The Stimulus System cannot generate enough control signals for proper SVX4 operation, so an interface board is needed to provide the additional control signals. These additional control signals are generated by the SVX4 adaptor board using an Altera [3] EPLD located on board to generate the extra control signals.

The adaptor board has multiple functions. It properly terminates the signal and bus lines of the SVX4 chip, contains test points which give convenient connection points for the flying-lead probe tips of the Logic Analysis System, and allows for dual mode (DØ/CDF) operation of the SXV4 chip. We show the SVX4 adaptor board in Figure 5.

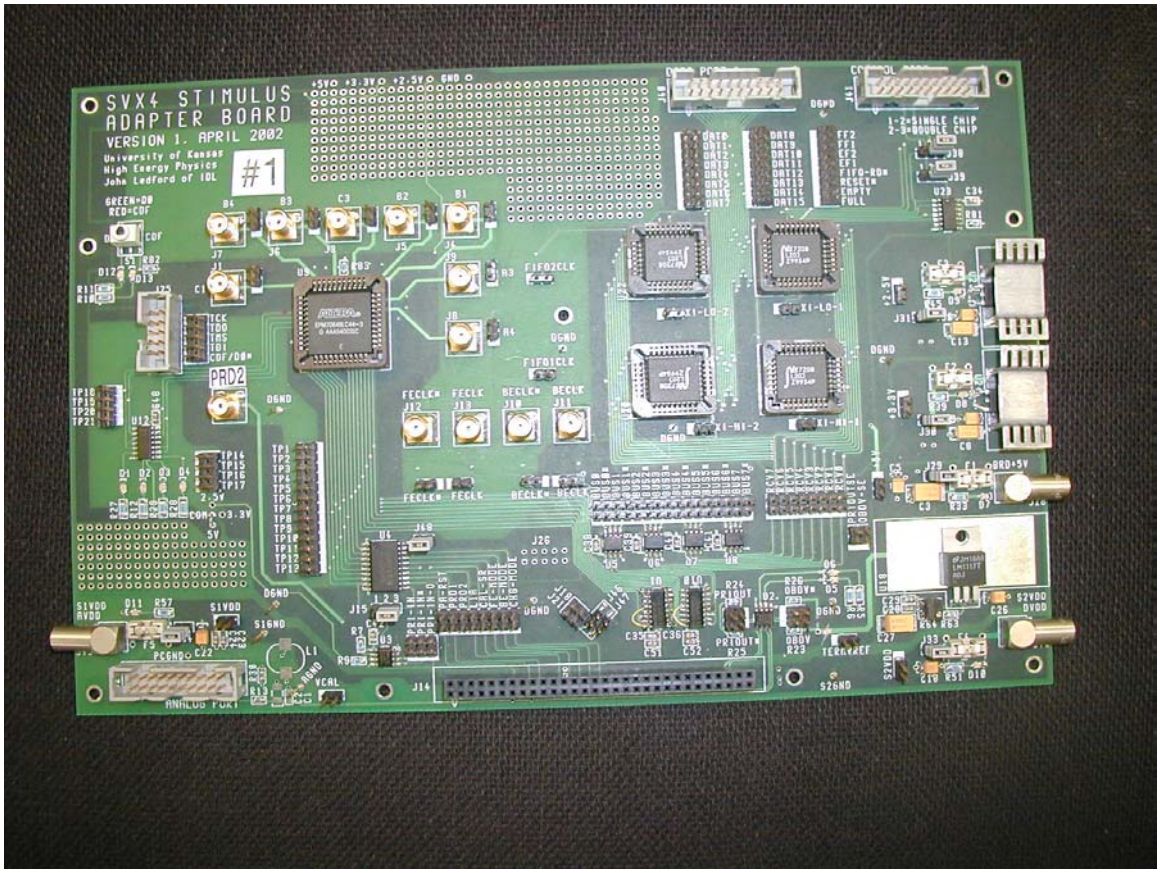

Figure 5: The SVX4 Adaptor Board. The adaptor board is used to interface the Stimulus System with the SVX4 chip. This board contains an Altera EPLD which contains a finite state machine used to generate the extra control signal for proper SVX4 operation. It also contains four FIFOs that are used to buffer data between the chip and the computer. The 60-pin connector in the middle of the bottom edge of the board is the connection used by the SVX4 chip carrier. The Lemo connectors at the sides of the board are used for power connections.

2.3 Probe Station

The adaptor board and chip carrier are mounted on a modified Rucker & Kolls [4] probe station with a Baush & Lomb MicroZoom [5] microscope used for visual inspection of the SVX4 die. The movable table contains mounts for the SVX4 adaptor board. The movable table can be closed which places the SVX4 chip carrier under the microscope and allows access for Picoprobes [6] by providing a stable base for the probes. The movable table is normally open to allow ample space for the cable connections coming from the Stimulus System to the adaptor board. We show a picture of the chip carrier and the adaptor board mounted on the movable table in Figure 6.

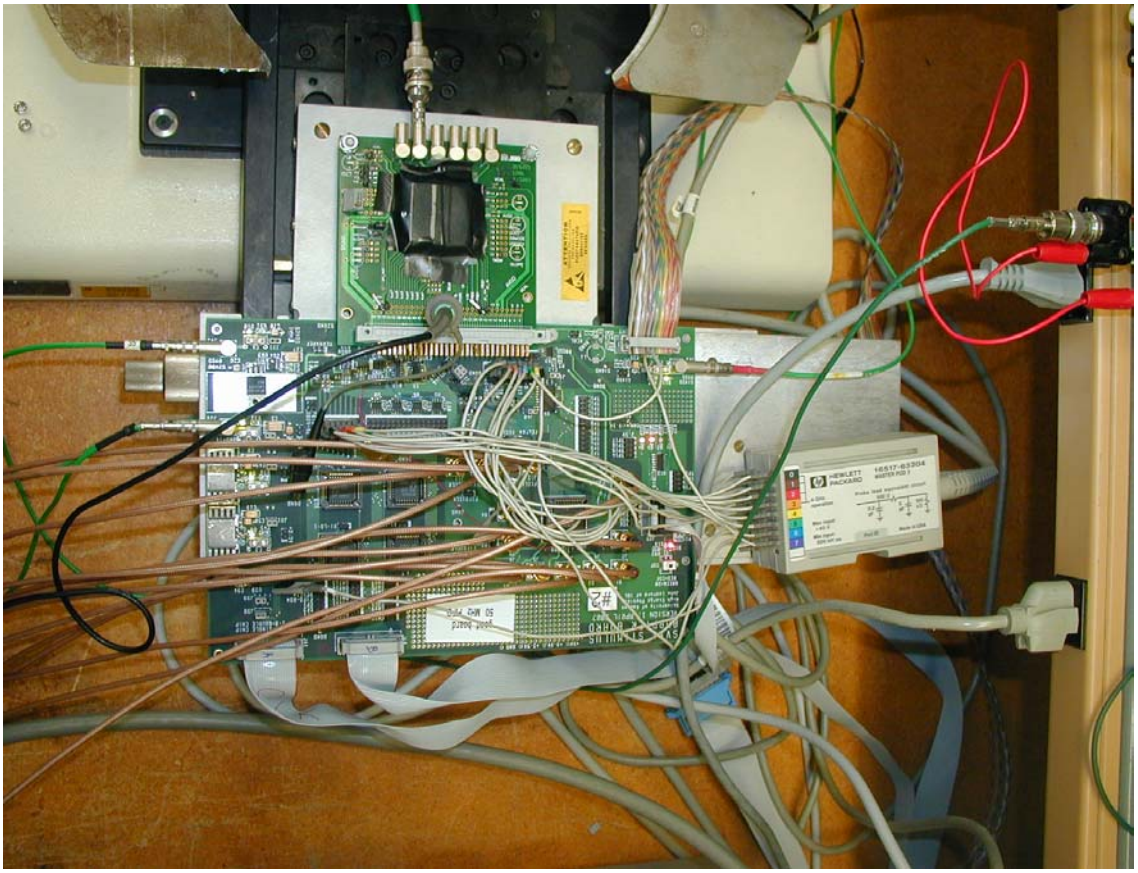

Figure 6: The chip carrier and SVX4 adaptor board mounted on the movable table of the Probe Station. The cables carrying the signals from the Stimulus System are shown to the left and the flying-lead probe from the HP pod connected to the Logic Analysis System is located to the right. The chip carrier is shown connected to the adaptor board and the SVX4 chip has a protective cover place on top of it to protect it from physical damage. The base of the Probe Station can be seen at the top of the picture and the U-shape base that the movable table slides underneath provides a stable base for the Picoprobes. Presently, the movable table is in the open position. The lower gray ribbon cables are connected to the PC.

2.4 The Tektronix HFS 9003 Stimulus System

The Tektronix Stimulus System [7] contains one HFS9DG1 differential output card and two HFS9DG2 single-ended output cards giving a total of 12 outputs. We list the outputs and their functions in Figure 7.

Stimulus System Output	Output Name	SVX4 (or Adaptor Board) Function
HFS9DG1		
Ch 1	FECLK	Front-end Clock
Ch 2	BECLK	Back-end Clock
Ch 3	BEMODE	Back-end Mode
Ch 4	L1A	Level 1 Accept
HFS9DG2		
Ch 1	CHMODE	Change Mode
Ch 2	CALSTR	Calibration Strobe
Ch 3	PRD2	Pipeline Read 2
Ch 4		Not Used
HFS9DG2		
Ch 1	PRD1	Pipeline Read 1
Ch 2	FEMODE	Front-end Mode
Ch 3	CONT	FSM Control
Ch 4	PARST	Preamplifier Reset

Figure 7: The name of the outputs from the Stimulus System and their function for the SVX4 chip and SVX4 adaptor board. BEMODE and L1A use only a single side of the differential output from the HFS9DG1 card. CONT is used as a clock for the finite state machine located on the SVX4 adaptor board and the SVX4 chip.

The Stimulus System generates the binary control patterns and sends them to the SVX4 through the adapter board. It has a maximum clock speed of 630 MHz. The frequency for normal operation is 530 MHz allowing an ability to change the waveform at the resolution of 2 ns. The Stimulus System has a total pattern memory of 64 K vectors permitting a pattern length of 128 μs. In practice, the pattern memory is divided into different cycles of SVX4 operation and these individual patterns can be repeated indefinitely.

2.5 HP 16500B Logic Analysis System

The HP 16500B Logic Analysis System [8] contains a 4 GHz/1 GHz Logic Analyzer along with a 2GS 32K Oscilloscope. The Logic Analysis System has two HP pods with flying-lead probe tips that are used to monitor the signals being sent to the SVX4 chip via the SVX4 adaptor board or the data output from the SVX4 chip. Each pod has 8 data lines which gives one the ability to monitor 16 different signals in the system. One probe is used to monitor control signals and the other is used to view the data from the SVX4 chip. The Logic Analyzer has a CRT which allows a user to graphically view the waveform being downloaded to the chip and the data coming from the chip.

3 Software

SVXEval is a custom written Windows 9x specific DAQ program coded in standard ANSI C. It uses drop down menus and dialog boxes to allow the user to control all the operating parameters of the SVX4 chip. It also has a full testing and analysis suite in

which the data can be taken and analyzed. A full description of how the SVX4 chip works and the specifications for chip operation are described in reference [1].

After powering up the SVX4 chip, it is necessary to download a serial bit stream to the chip through the signal PRI_IN or Priority In which is gated by the front-end clock while the chip is in the initialization cycle established by the change mode (CHMODE), front-end mode (FEMODE), and back-end mode (BEMODE) signal lines.
The 191 long bit stream consist of a 128 long channel mask with dual functionality: it acts as a mask for charge injection during calibration and it acts as a way to disconnect problematic channels from preamplifier inputs in normal operation.

The remaining 63 bits in the initialization bit stream are used to set the operating parameters of the chip. The dialog box in the SVXEval program used to set all operating parameters for the front-end and back-end shown in Figure 8.

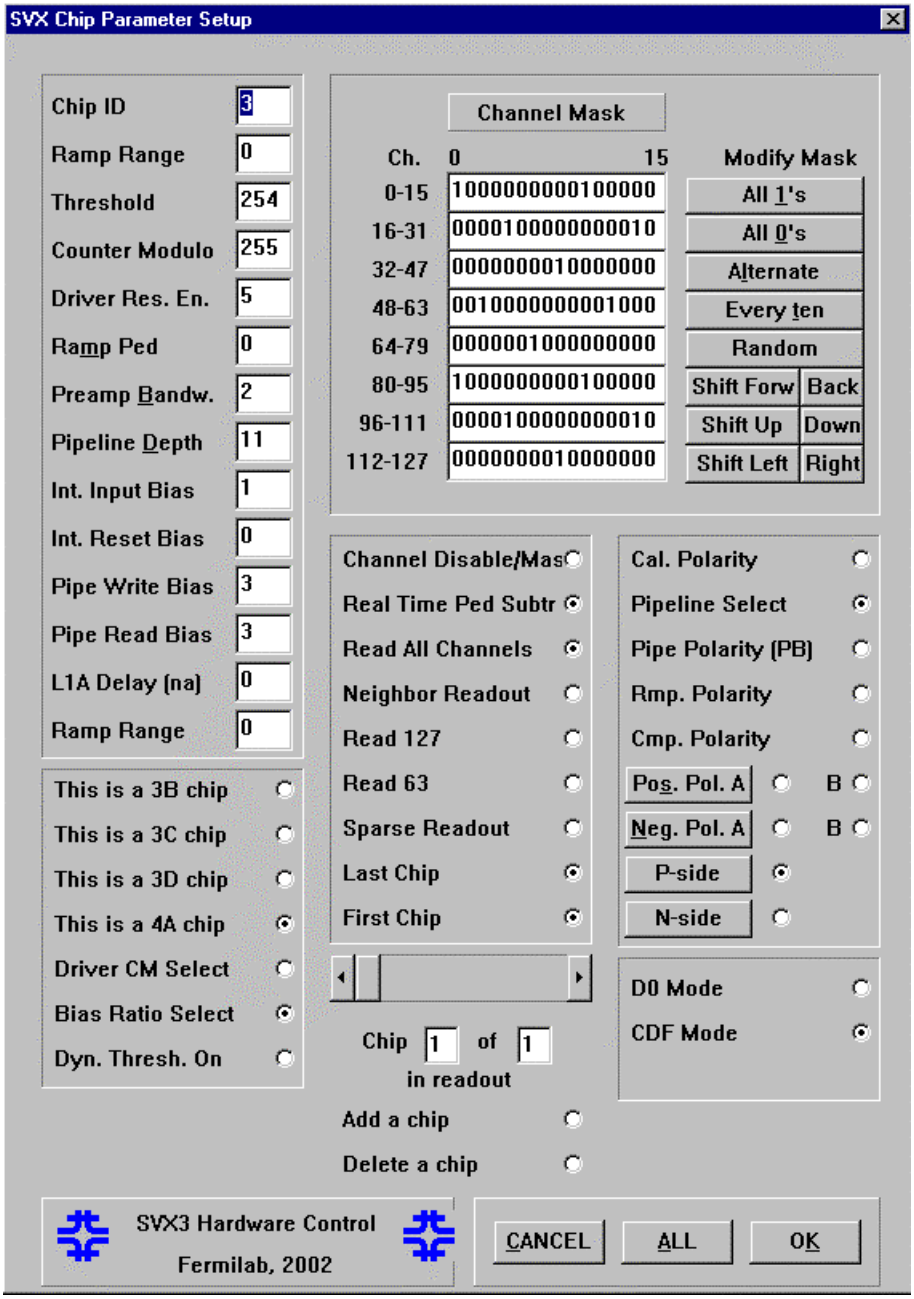

Figure 8 Dialog box containing all the operating parameters that will be downloaded to the SVX4 chip for normal operation. This upper right corner shows the 191-bit stream that is downloaded to the chip. The other parts of the menu show the additional operating parameters that are set and the modes of the chip that can be chosen.

The waveforms that are downloaded to the chip are generated algorithmically and can be altered by a graphical waveform display/editor provided by the software. We show the waveforms for the DØ mode and CDF mode of the SVX4 chip in Figure 9 and Figure 10, respectively. In Figure 11, we show the data output from the SVX4 chip for various pedestal.

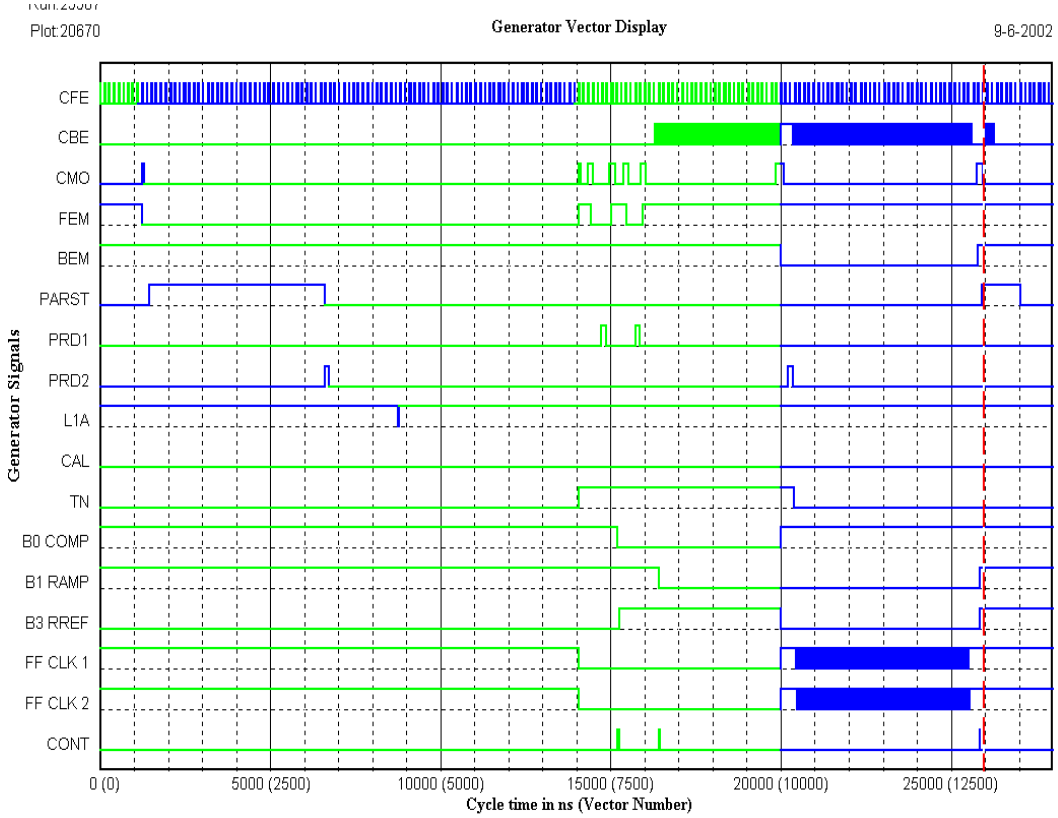

Figure 9 Control pattern for the DØ mode of operation for the SVX4 chip.

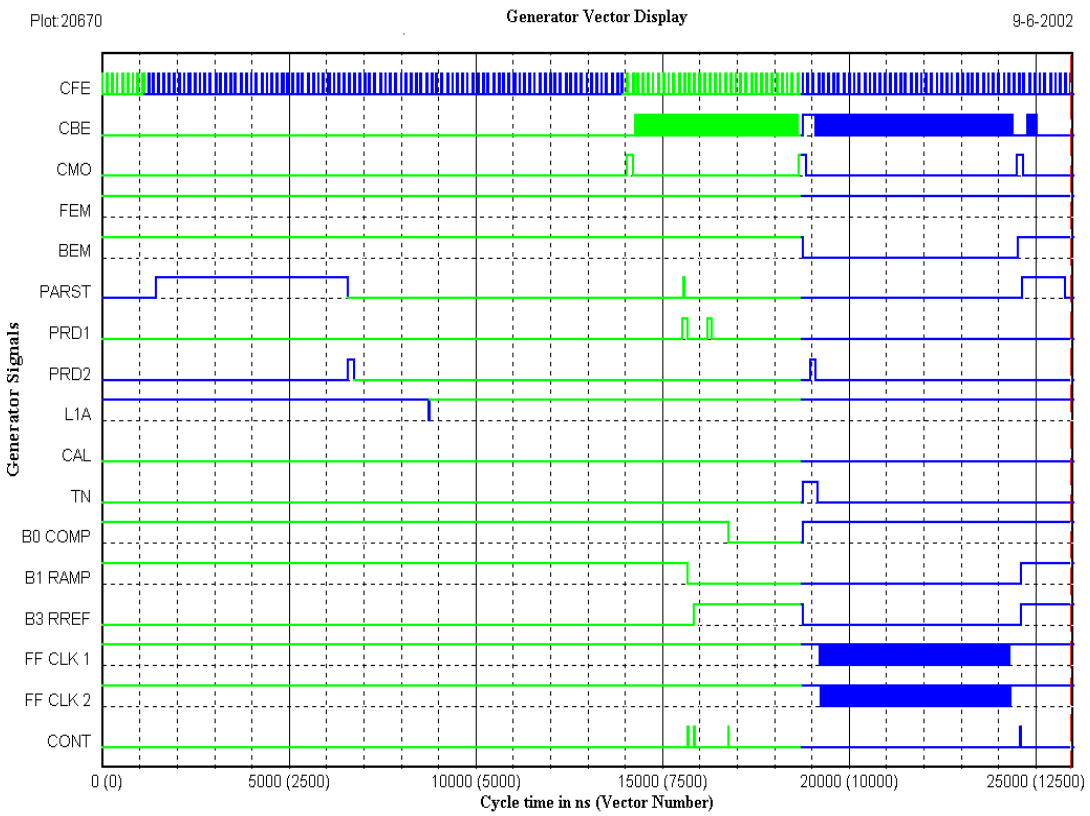

Figure 10 Control pattern for the CDF mode of operation for the SVX4 chip.

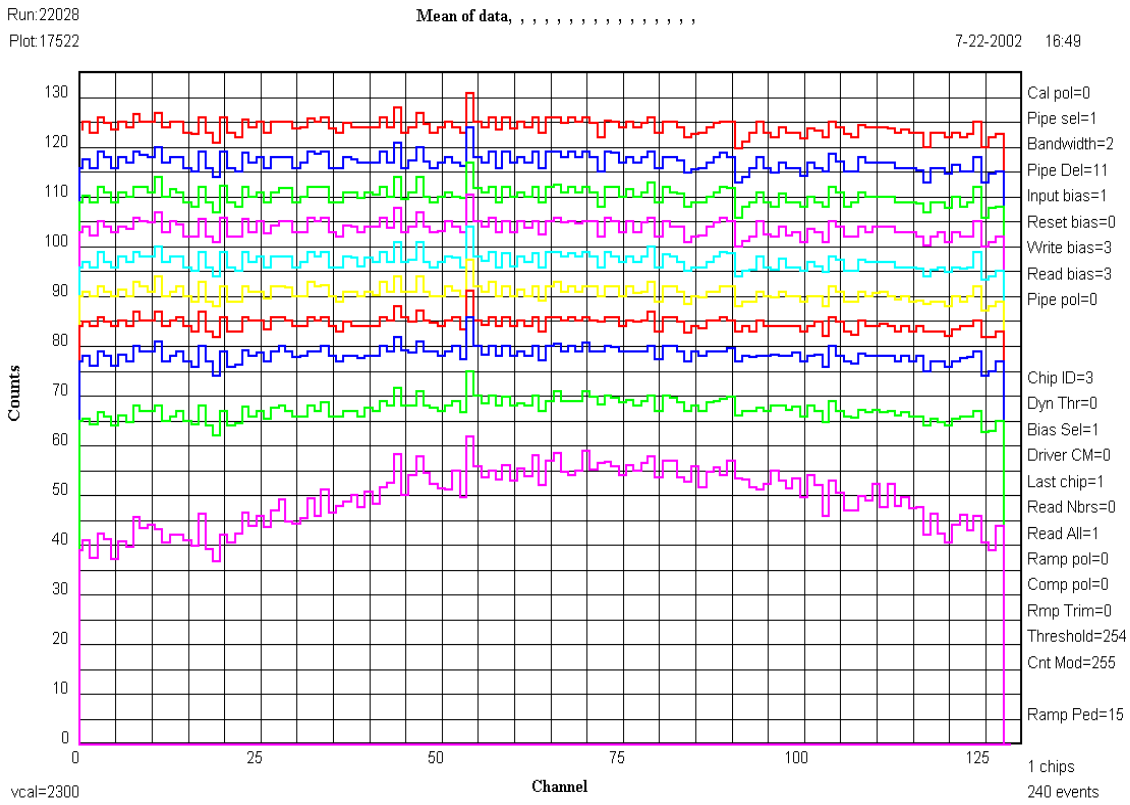

Figure 11 Pedestal scan for the SVX4 chip as a function of channel number in read all mode.

4 References

[1] L. Christofek *et al.*, "The SVX4 User's Manual", DØ Note 4252.
[2] http://www-cdf.lbl.gov/users/mweber/svx4/
[3] http://www.altera.com/
[4] http://www.ruckerkolls.com/
[5] http://www.bausch.com/
[6] http://www.ggb.com/
[7] http://www.tektronix.com/
[8] http://www.hp.com/