Preliminary Test Results for the SVX4

L. Christofek, K. Hanagaki, P. Rapidis, M. Utes

Abstract: We present and summarize the preliminary test results for SVX4 chip testing.

1 Introduction

There are presently two versions of the SVX4. Version 2 has on-chip bypassing and Version 1 does not. The on-chip bypassing is a layer of transistors under the front-end analog pipeline that acts as a bypassing capacitor for the voltage supply. Its size is about a microfarad. We aggressively choose to test Version 2 because of this feature.   The feature is advantageous for hybrid design because it eliminates the need for an additional passive component on the hybrid itself by placing it on the actual SVX4 die.

Also, the SVX4 was designed to operate in two modes: D∅ and CDF. One can set which mode the chip will operate by placing a jumper in the proper position on the SVX4 chip carrier. In either mode, the chip can either use the operating parameters from the shift register or the shadow register. Similarly, this is selected by placing a jumper on the SVX4 chip carrier. This chip has this feature because it was unknown whether the new design of the shadow register would be operable. The shadow register is also call the SEU register or Single Event Upset register. An introduction into the functionality of the chip and an explanation on the difference between D∅ and CDF mode can be found in the SVX4 User's Manual [1].

2 Experimental Setup

Most of the results reported in this paper come from the Stimulus Test Stand. The test stand is presently located at Wilson Hall on the fourteenth floor. Detailed descriptions of the Stimulus Test Stand and the PATT03 test stands can be found elsewhere [2,3].

3 Gain

In order to measure the gain, we wire-bonded four channels of the chip to four different valued external capacitors. We then injected an external pulse into these channels using a Hewlett-Packard 8112A Pulse Generator. The external pulse passes through a variable attenuator to reduce its amplitude into the μV range (larger pulses will destroy the amplifier input and channel). We can control the pulse height of the signal in two independent methods: 1) varying the pulse height of the pulse generator (mV~V) and 2) varying the attenuator (10~100 dB). The injected charge is then calculated by using

$$Q = C_{ext} \times V_{pulser} \times \text{-20} \log_{10} (V_{cap}/ V_{pulser})$$

where Q is the total charge injected, C_{ext} is the external capacitance bonded to the channel, and $\text{-20} \log_{10} (V_{cap}/V_{pulser})$ is the attenuation factor [dB] with V_{cap} being the actual voltage the external capacitor sees and V_{pulser} being the output voltage of the pulser.

After injecting the pulse into the channel, we measure the ADC output of the channel. We then take the difference, Δ, between the ADC output of the injected signal and the ADC output of the pedestal. The gain, G, is then calculated by

$$G \equiv Q / \Delta .$$

In Figure 1, we give a cartoon schematic showing the experimental setup.
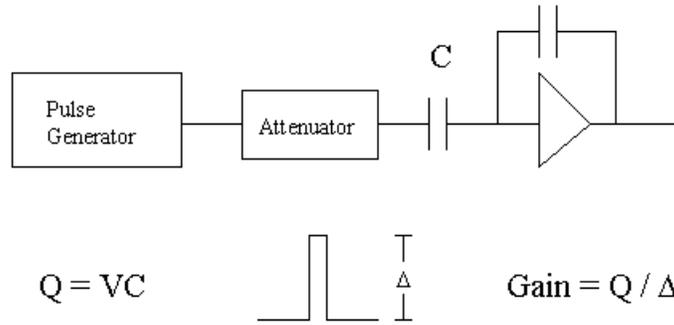
Figure 1 Cartoon schematic of the experimental setup used to measure the gain of the SVX4 chip. An external pulser generates a pulse that passes through an attenuator, which is then injected into an external capacitor wire-bonded to a single channel of the SVX4. The charge injected can be calculated from Q=VC. The gain is then calculated by measuring the difference between the charge injected signal and pedestal and dividing that quantity into the total charge injected. This gives the number of electrons per ADC count.

Because the SVX4 uses double correlated sampling, it is very important to setup the correct timing of the injected pulse. In simple terms, the preamplifier output is sampled during the falling edge of the front-end clock and then sampled again at the next rising edge of the front-end clock and the difference is taken as the signal to be digitized (this is the operational definition of double correlated sampling). It is therefore important to inject the external pulse directly after the falling edge of the front-end clock to allow the maximum integration time possible [4]. We show the results in Table 1 and Table 2. Unless otherwise stated, all results were obtained using the digitization frequency of 53 MHz and a readout frequency of 26.5 MHz.

BW\C	10 pF	33 pF	68 pF
0	706	899	1332
6	733	1119	1756
15	860	1561	2575

Table 1 Measured gain in terms of the number of electrons per ADC count. We measured the gain as a function of three different bandwidth values. The above data is for a Version 2 chip is D∅ mode. This data was taken using a ramp slope setting equal to 1. A decimal value of 1 means that the least significant bit of this parameter was set to 1.

BW\C	10 pF	33 pF	68 pF
0	682	1023	1246
6	706	1262	1756
15	824	1854	2146

Table 2 Measured gain in terms of the number of electrons per ADC count. We measured the gain as a function of three different bandwidths values. The above data is for a Version 2 chip in CDF mode. This data was taken using a ramp slope setting equal to 1. A decimal value of 1 means that the least significant bit of this parameter was set to 1.

The gain can also be measured by using the internal calibration injection circuitry. By injecting a calibration pulse on a channel that is not bonded out through an external capacitor, the number of ADC counts per mV can be calculated for a specific bandwidth setting. Assuming an input capacitance of 25 fF for the calibration injection capacitor, we calculated a gain of 591 electrons per ADC count. The results are shown in Table 3. This is approximately a 13% difference from using the external pulser method.

mV	0	30	77	125
ADC counts	142.8	150.8	163.5	175.2
Δ [counts]	0	8.0	20.7	32.4
mV/Δ	-	3.75	3.72	3.86

Table 3 Measured values for the ADC output as the calibration injection voltage is varied. The value of ramp slope was set to 1 and the bandwidth was set equal to 0. The difference between any two values can be used to calculate the value of mV per ADC count. The average value is 3.78. The above data is for a Version 2 chip in CDF mode.

4 Noise

Using the measured gain from above, the RMS of the pedestal can be converted into the number of electrons also known as the equivalent noise charge (ENC). We show this in Figure 2. This measurement includes contributions from the front and back-end of the chip as well as any common mode noise contributions that may be present in the system. We then fitted the data using the data analysis package in EXCEL. The results are shown in Table 4.

Equivalent Noise Charge
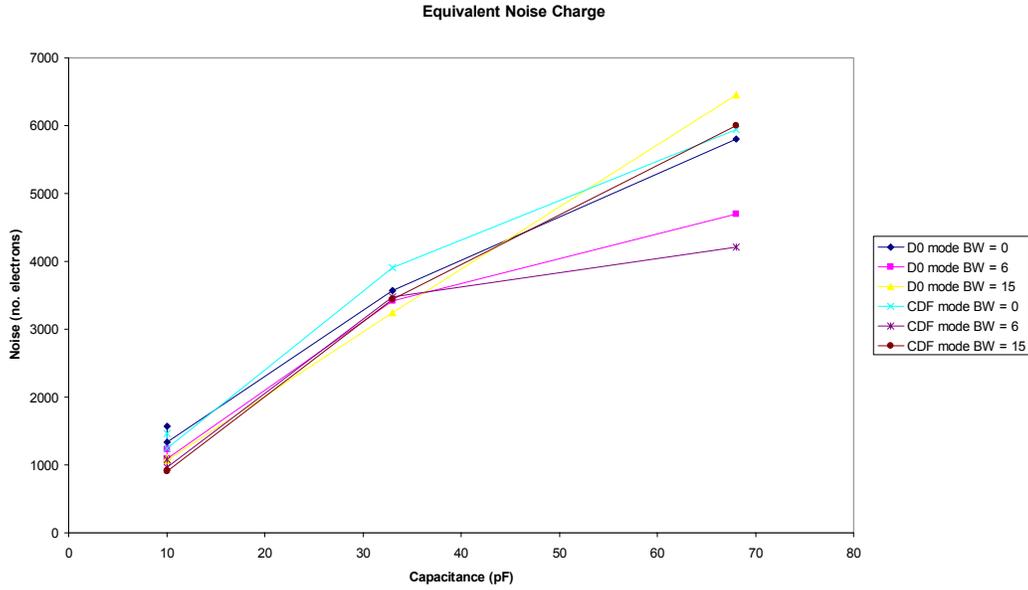
Figure 2 Plot of the equivalent noise charge (ENC) as a function of capacitance in both D∅ mode and CDF mode for three different bandwidth settings. We used a Version 2 chip with three different valued capacitors (10 pF, 33 pF, and 68 pF).

	D∅ mode	CDF mode
BW = 0	$715.9 + 80.08 \times C$ [pF]	$786.8 + 75.51 \times C$ [pF]
BW = 6	$728.5 + 56.41 \times C$ [pF]	$736.9 + 62.00 \times C$ [pF]
BW = 15	$140.9 + 88.48 \times C$ [pF]	$166.8 + 92.65 \times C$ [pF]

Table 4 The ENC for bandwidths settings of 0, 6, and 15 obtained from a linear fit to data in both D∅ mode and CDF mode.

5 Rise Time

This current chip submission has several test pads on the chip for detailed studies. Channel 127 has a special probing pad on top of the chip in which we can study the preamp output. This pad allows direct measurement of the rise time of the preamplifier. We used a P6243 Tektronix FET probe. It is important to note that the output buffer has to be correctly biased before the output can be measured. We biased the PMOS output using a 5.92V power supply through a 1 kΩ resistor.

We used a Version 2 chip in CDF mode to measure the rise times using an external calibration injection pulse with a magnitude of 2.4 V and a large pulse width (τ >250 ns). The injection capacitance for the channel was 10 pF. The output from the preamplifier is shown in Figure 3. The results for the rise time using the 10-90% definition are given in Table 5.
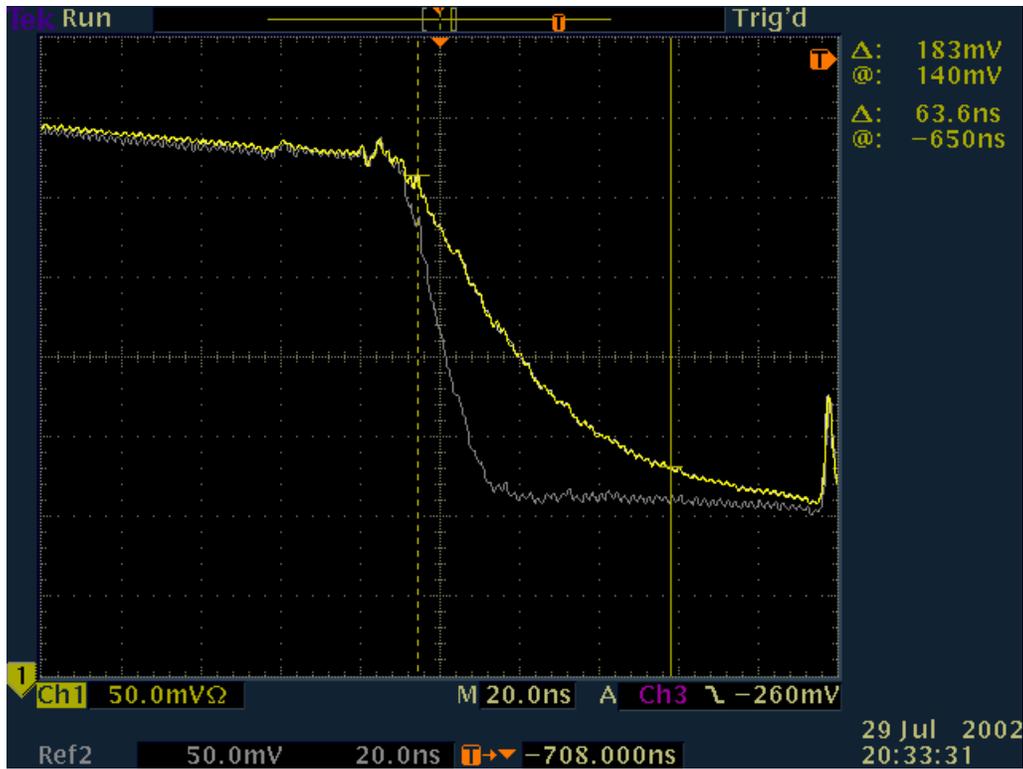
Figure 3 A picture of the preamplifier output showing the rise time of channel 127. The yellow line corresponds to a bandwidth setting of 15 and the white line corresponds to a bandwidth of 0. The spike at the far right of the picture is pick-up from the front-end clock.

Bandwidth	10 pF load
0	20 ns
3	32 ns
7	46 ns
11	58 ns
15	64 ns

Table 5 The measured rise times of the preamplifier using the 10-90% definition of rise time for various bandwidth settings. They were made using channel 127.

We also used this same configuration as above to measure the reset time of the preamplifier. In Figure 4, we see the reset of the preamplifier. The reset has a slight overshoot, but the value we measure for the reset time is 17.97 ns.
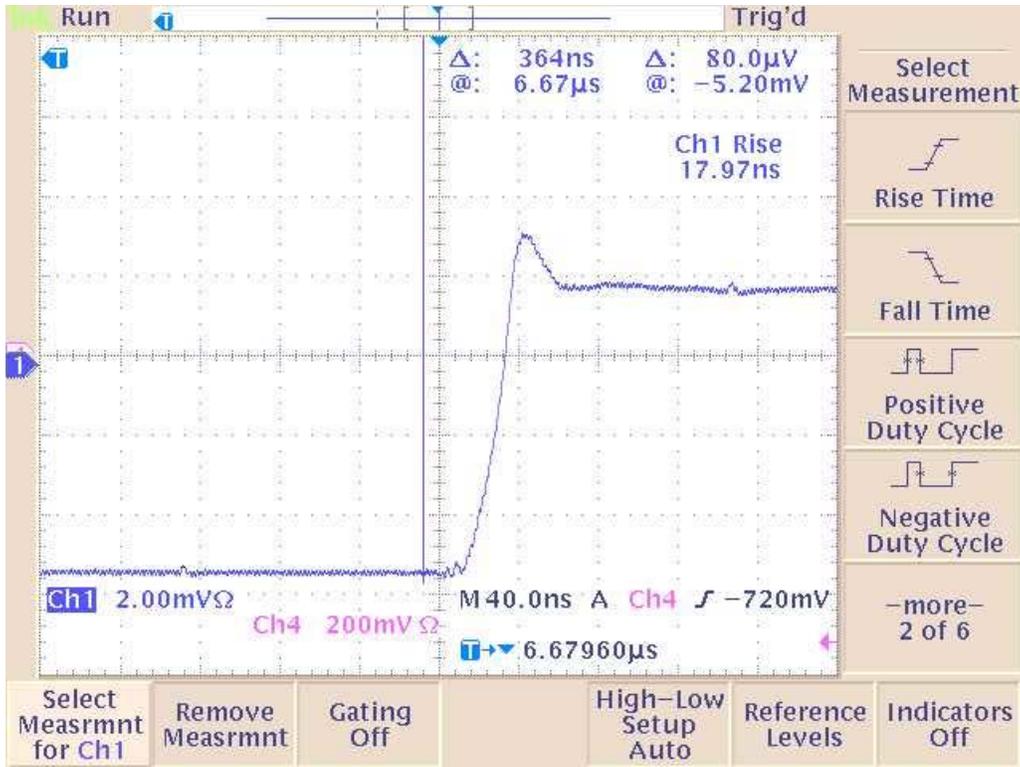
Figure 4 Screen shot from an oscilloscope showing the preamplifier reset in action.   This was taken from channel 127.

6 Probing the Ramp

The ramp can also be investigated because it has test pads that allow direct observation. In Figure 5, we show the actual ramp in action from a Version 2 chip. We measured the ramp slope using the FET probe mentioned above. Table 6 shows the measured slope and the design values. In the design, the slope is determined from

$$0.5 \text{ mV/ns} \times [\ 1 + (\ 2 \times R0\ ) + (\ 2 \times R1) + (\ 1 \times R2\ )\ ]^{-1}$$

where R0, R1, and R2 correspond to each bit setting.

We confirmed the functionality of the ramp pedestal settings (a four bit field) by downloading all values of the pedestal and then measuring the pedestals using the chip's ADC. We did the analogous thing for the ramp range settings using a single ramp pedestal setting. We show the output of the ADC for both studies in Figure 6.
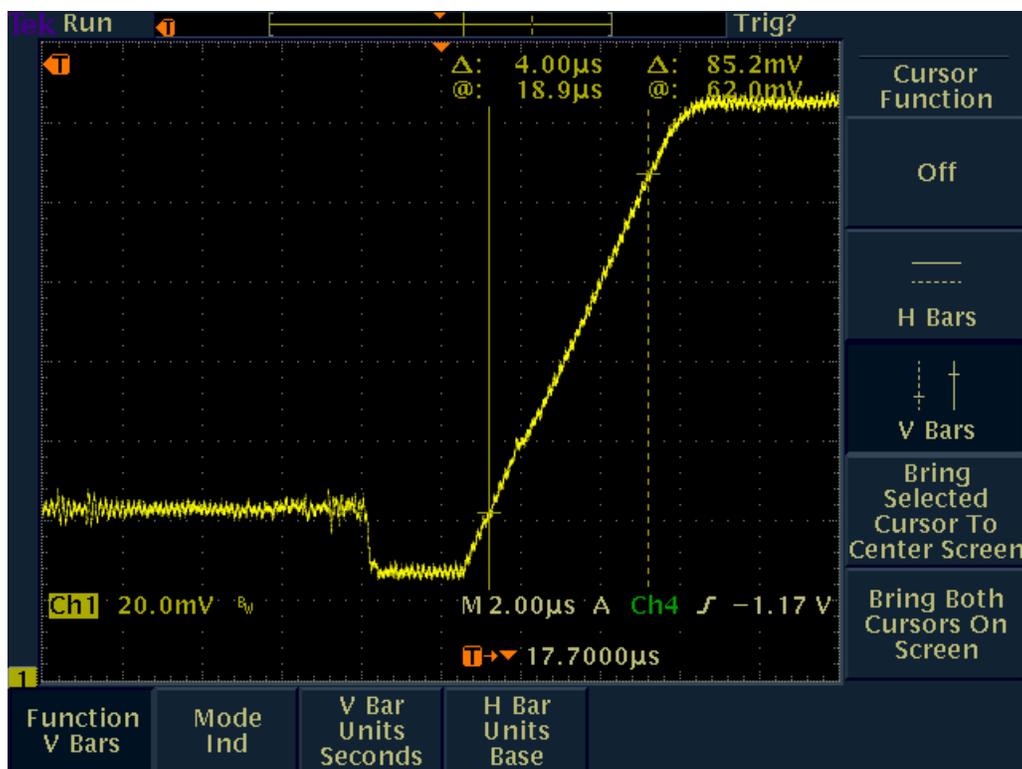
Figure 5 A picture showing the actual ramp for a Version 2 chip. We used the oscilloscope's functions to measure the ramp slope.

Ramp Range Setting	Bit Pattern	Design (mV/ns)	Measured (mV/ns)
0	000	0.500	0.416
1	001	0.167	0.149
2	010	0.167	0.137
3	011	0.083	0.082
4	100	0.250	0.337
5	101	0.125	0.111
6	110	0.125	0.105
7	111	0.083	0.073

Table 6 Ramp Range settings with the bit pattern - listed in R2, R1, R0 order - along with the design and the measured values for the ramp.
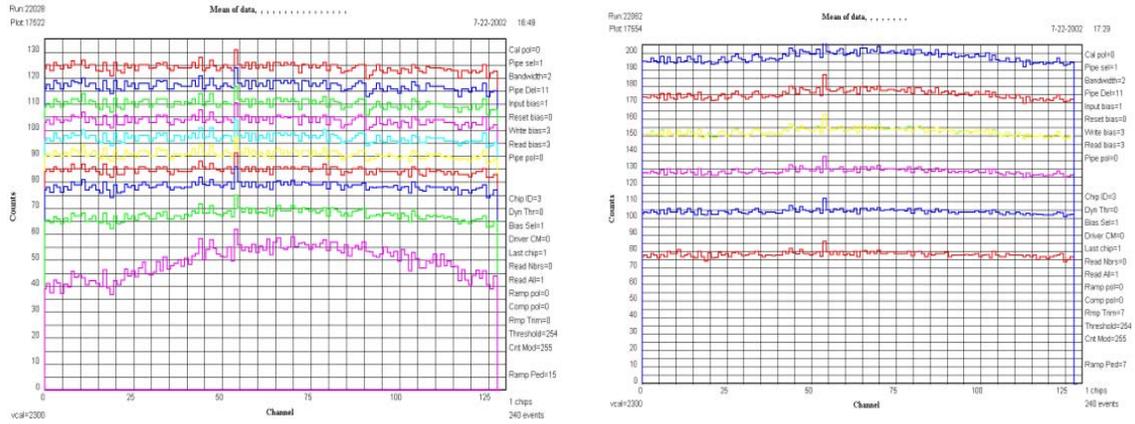
Figure 6 The left histogram shows a pedestal scan from the SVX4. The right histogram shows a ramp range scan. The pedestal scan only includes settings from 0-9. Higher settings give pedestals of zero.

6.1 Pedestals as a Function of Digitization Frequency

The SVX4 chip is extremely fast when digitizing. During digitization, any back-end clock edge seen by the chip will count as an ADC count. The pedestal value is downloaded to the chip, but this value depends on the frequency of the back-end clock. In order to compare with simulation and to see how fast the chip can actually digitize, the digitization clock frequency was increased as high as possible while locking the readout frequency. The results are shown in Figure 7.

**Pedestal versus Digitization Frequency**
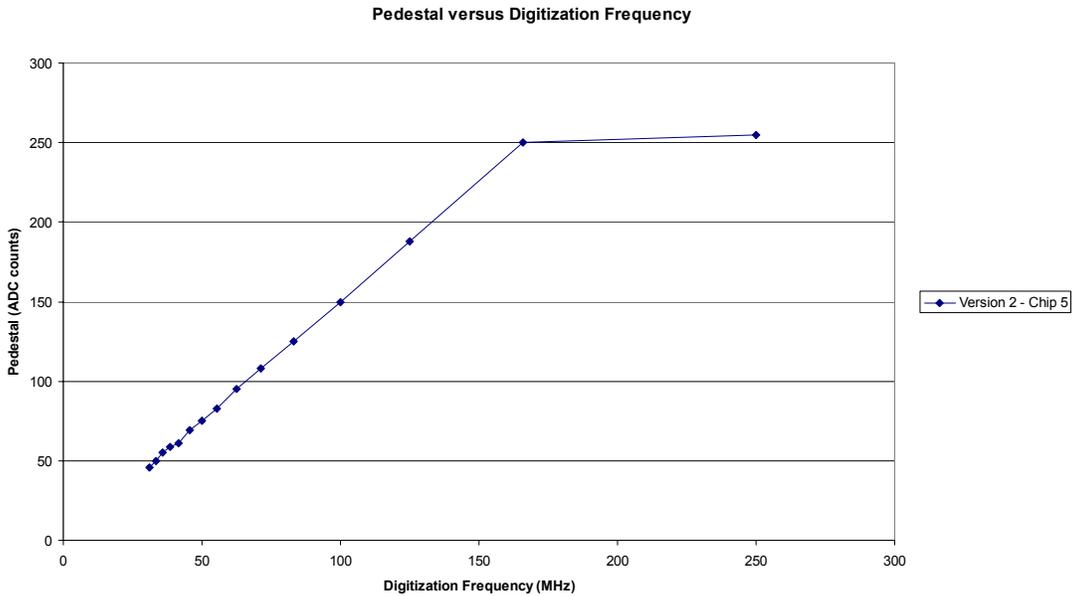
Figure 7 Pedestals as a function of the digitization frequency for a Version 2 chip. The readout frequency of the chip is locked at 25 MHz. The linear increase is expected from theory. As the clock gets faster it hits the full scale before the ramp equals the pipeline output. This is evident for frequencies above 150 MHz.

6.2 Variations from chip to chip

We were also interested in studying how much the settings for the pedestal and the ramp varied from chip to chip in order to study process variations. We had five individual SVX4 chips mounted on chip carriers. We performed a ramp range scan and a pedestal scan to measure the variations between chips. In Figure 8, the value of the pedestal is shown for different values of the ramp range that were downloaded. The structure seen is due to the weighting scheme used in adjusting the slope of the ramp. The formula was given in Section 6.
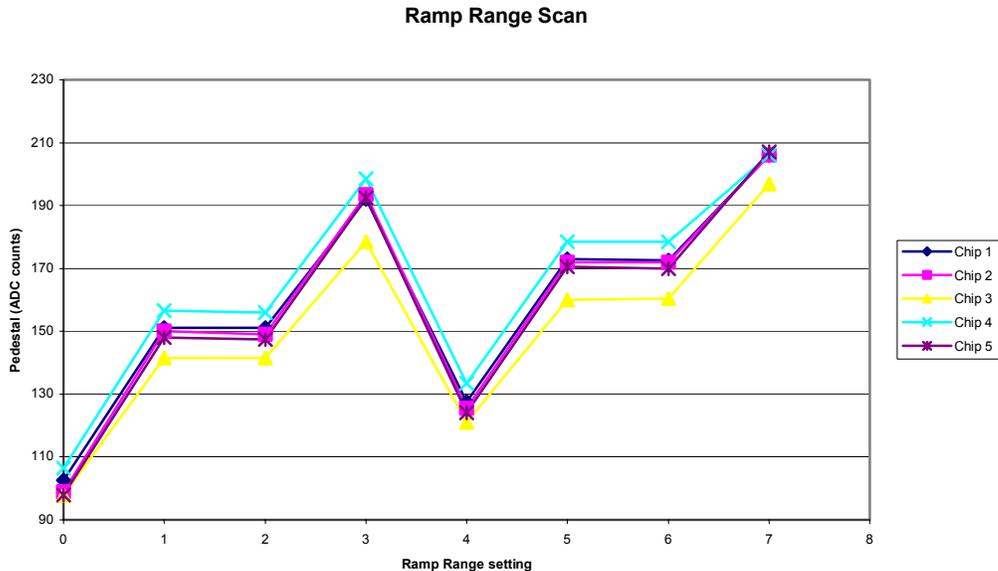

Figure 8 Ramp range scan showing the value of the pedestal as a function of the value downloaded for the ramp. This plot shows that even though ramp range is a three bit field allowing seven values, two values give the same pedestal therefore only giving five different values with the slope with the chosen external resistor on the chip carrier.

In Figure 9, we converted Figure 8 into a plot of the pedestal as a linear function of the ramp slope. This shows the linear nature of the pedestal for different values of the slope. We observed up to a 7.5% difference from chip to chip.

We also measured the variation of the pedestal as a function of the ramp ped setting. This is shown in Figure 10. We can see the linearity up to ramp ped setting of 7. The non-linearity is due to the pedestal bowing [5]. We observed up to an 11% variation for the pedestal settings. Both of these studies were done with a fixed digitization and read out frequency.
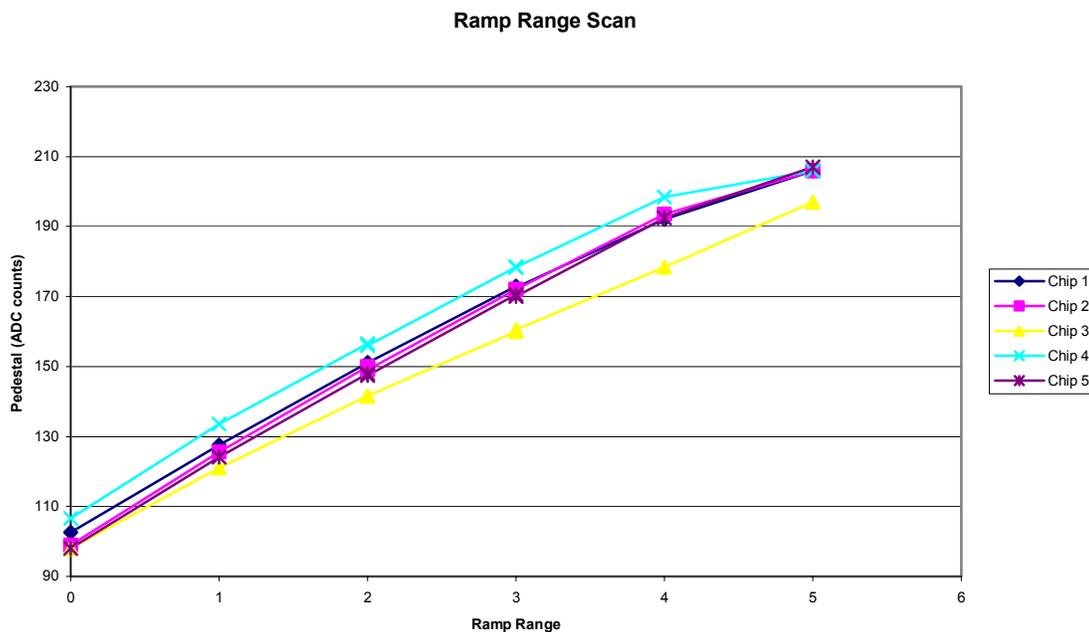
Ramp Range Scan

Figure 9 Pedestals as a function of the ramp range slope. The conversion is implicit in the histogram. This shows the linear nature of the slope versus the downloaded value of the ramp range value.
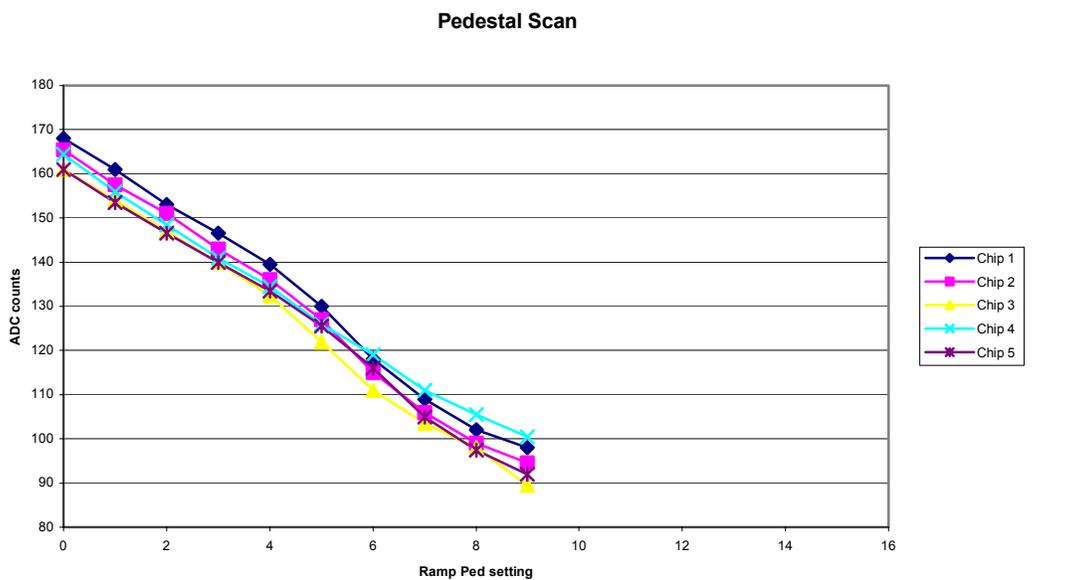
Pedestal Scan

Figure 10 Pedestals as a function of the ramp ped setting. Ramp ped is the variable that downloads the pedestal. The values for the pedestals are slightly non-linear above a setting near 7. This is due to the pedestal bowing discussed in the text. Values higher than 9 give a value of zero for the pedestal.

7 Linearity

We studied the linear response of the channels by injecting a known amount of charge in increments and then monitoring the ADC output. Figure 11 shows the ADC output of a five individual channels of the SVX4 as a function of the calibration injection voltage. In order to measure the non-linearity, we fitted this data to a straight line and then plotted the deviation from the predicted value. We show the results of this procedure in Figure 12. We see from Figure 12 that the greatest deviation was on the order of 1% and that occurred when the injection calibration voltage was zero.
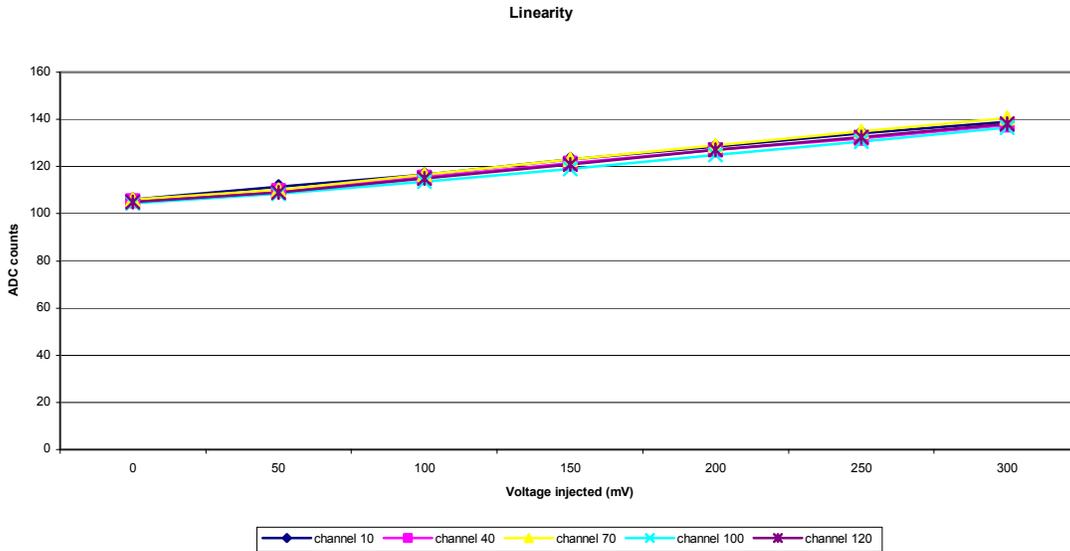

Figure 11 ADC output as a function of the calibration input voltage for five independent channels of the SVX4 chip.
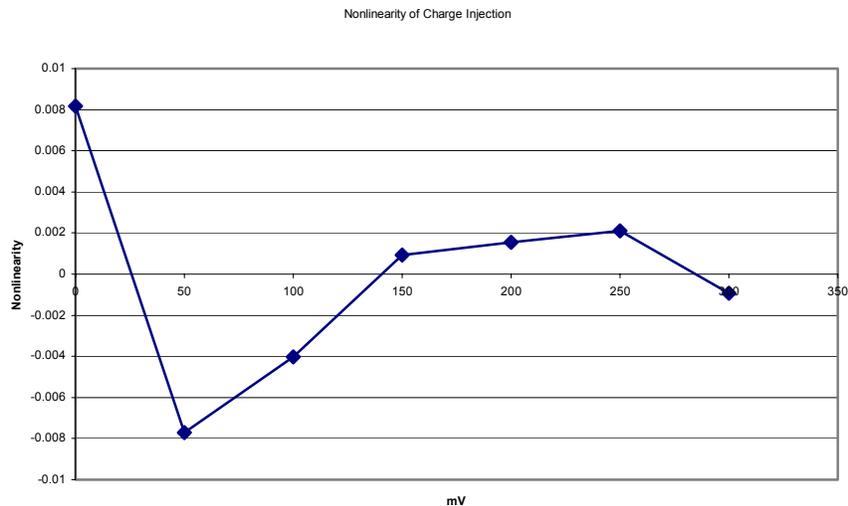

Figure 12 The non-linearity of the ADC output as a function of the calibration injection voltage for a single channel. The largest deviation from the straight line fit occurs when there is no charge injection. It is of the order of 1%.

8 Current Consumption

Because the Stimulus System uses single chips on a chip carrier, we were able to measure the current consumption of the SVX4 using an AM 503 Current Probe Amplifier. The current probe uses the Hall Effect to measure the magnetic field of the cables that carry current. The current probe was calibrated using a 5V supply voltage and a 200 Ω resistor. Expected and measured currents were 25 mA and 24 mA, respectively. To measure to currents separately or summed, a single cable was attached to the power supply with the least ripple, then subsequently teed and connected separately to AVDD and (SVDD+DVDD).

Only one Version 2 chip was measured in CDF mode. We measured the currents for AVDD and DVDD separately and then combined. Also, the SVX4 currents were measured for a variety of chip settings and bias voltages. There was a small dependence on chip output driver current and a dramatic dependence on chip bias. The latter will have a major impact on requirements for low-voltage power supplies.
Data was acquired using single-event read all runs in CDF mode with a calibration pulse injected on every 10th strip.   Separately measured currents agreed with their sum to within a few percent. Currents measured in different runs also agreed to within a few percent. Because we used an unsaturated cal inject on every 10th line, SVDD current may not have been maximized during readout.

Figure 13 shows AVDD and (DVDD+SVDD) currents measured separately as well as the sum. Bias at the chip carrier was 2.44V. A green line found in all figures is the trigger signal that was used the trigger the oscilloscope. In Figure 14, we see the shape of AVDD as a function of time. The jump in the current is when the chip entered the acquire cycle. The shape of AVDD is believed to be from the following. When then chip is not acquiring data and neither the preamp reset or the front-end clock are not held high, the chip enters a saturation state as demonstrated by the long tail in AVDD. It is believed that the current would stay constant before and after the data acquire cycle if the preamp reset and the front-end clock were held high.

The output driver was varied over its maximum range from id=1 (smallest current) to id=7 (largest current). The AVDD current was constant, but the (DVDD+SVDD) current varied by almost 20% as shown in Figure 15.

Finally, total SVX4 current as a function of bias voltage is displayed in Figure 16. The current increases approximately by a factor of two between bias voltages of 2.25V and 2.75V. The bias was measured at the chip carrier; supply voltages were higher by a few hundreds of a Volt.

Though more investigation is required, hybrid currents required probably consist of the peak above wings added to the total current after readout multiplied by the number of chips. For a 10-chip hybrid, that would be (126 mA * 10) + 24 mA = 1.5 A. To test this interpretation, the currents will be measured on a 2-chip hybrid.
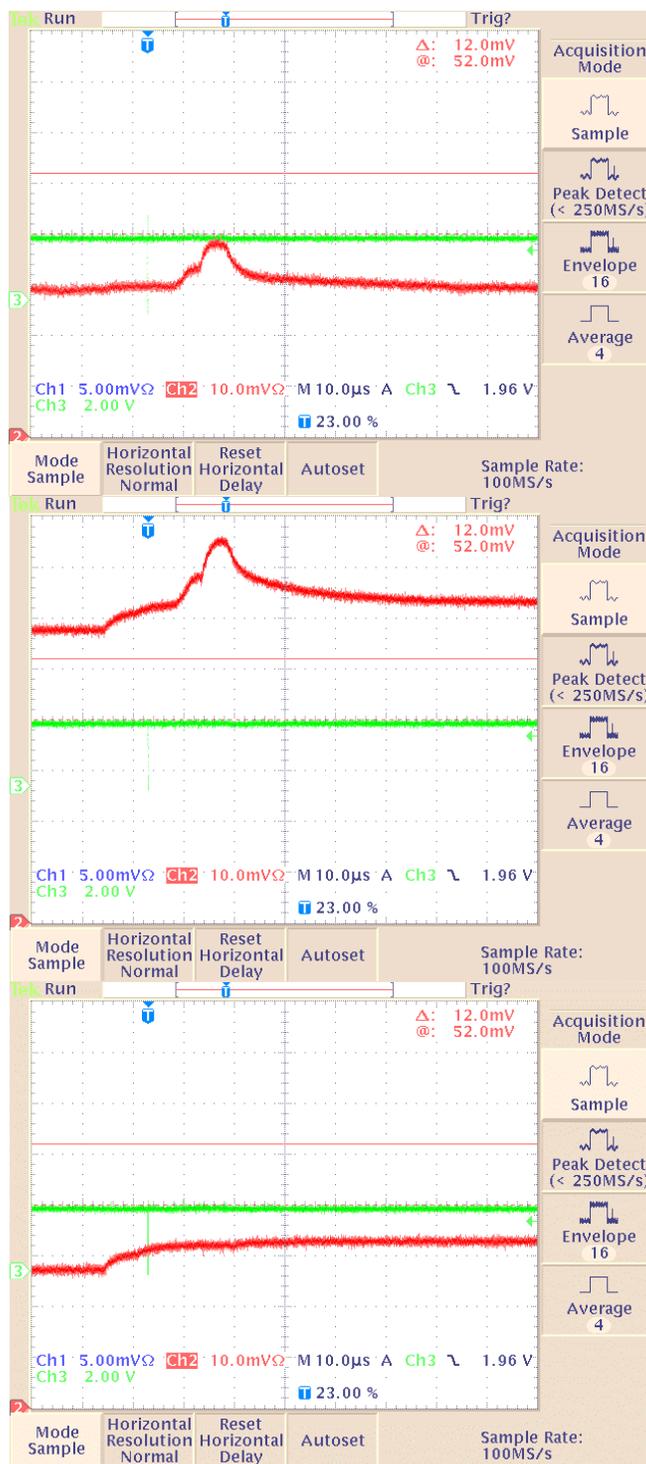
Figure 13 Measured currents from AVDD, (DVDD+SVDD) and the combined voltage supplies are shown on the top, middle, and bottom, respectively. The vertical scale is 20 mA/division and the zero is at the lower left-hand corner. The peak on (DVDD+SVDD) is probably due to readout. Individual currents add to the total current with a few percent.
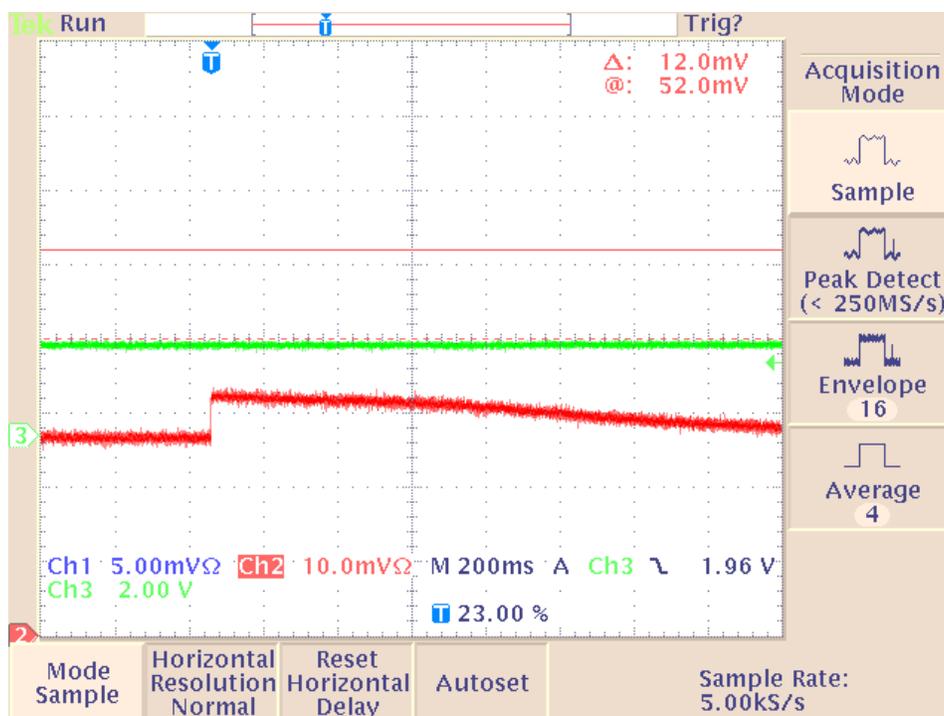
Figure 14 AVDD versus time. The vertical scale is 20 mA/division, with the zero indicated by the red arrow at the lower left-hand corner. The horizontal scale is 200 ms/division. The explanation of the shape is discussed in the text.
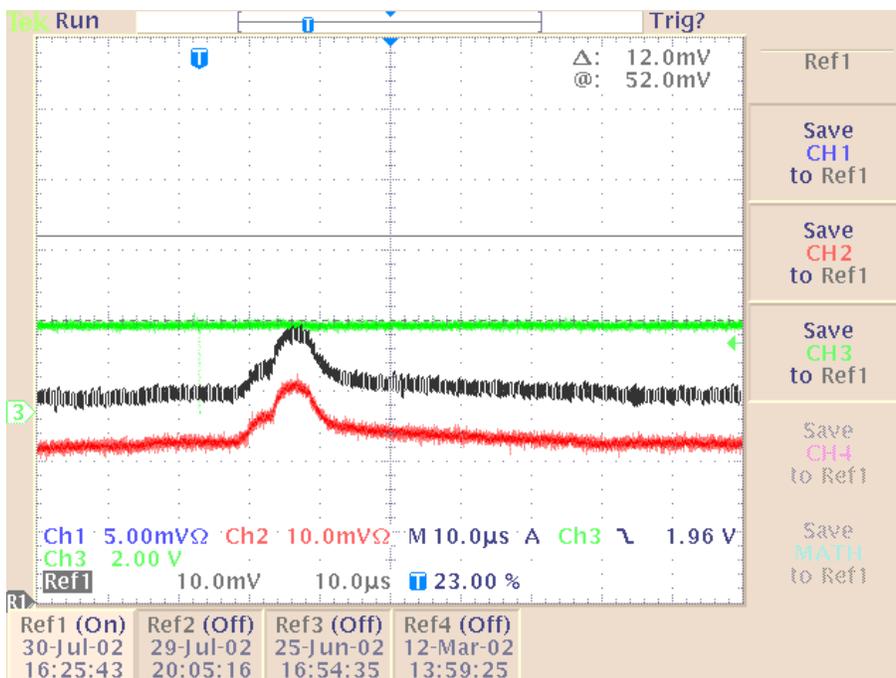
Figure 15 DVDD currents measured as a function of time at 10 μs/division. The higher (black) curve is for id=7 (maximum output driver current), while the lower (red) curve is for id=1 (minimum output driver current). One major vertical division corresponded to 20 mA, and zero was at the lower left-hand corner. Peak currents were 76 and 62 mA, respectively.
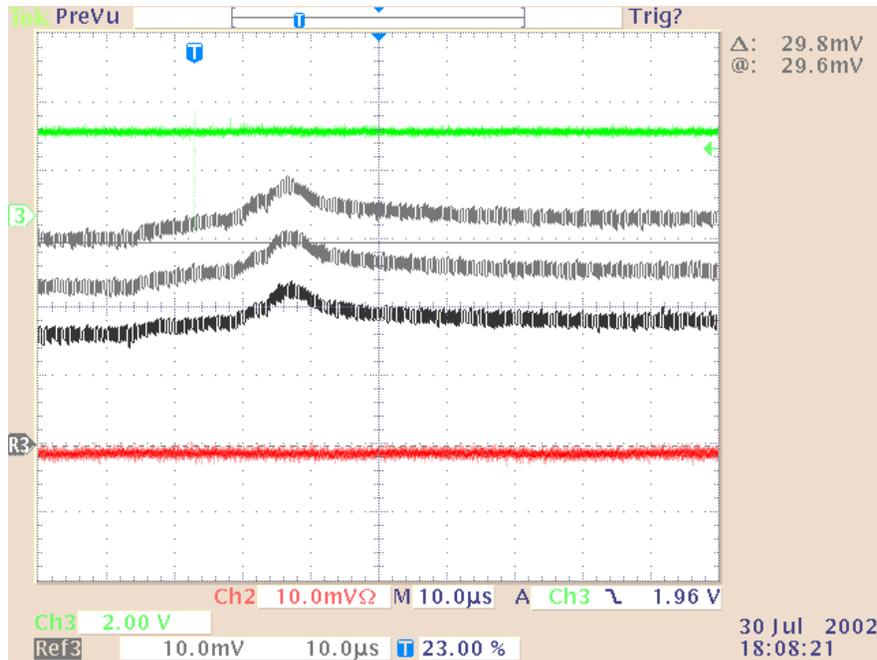
Figure 16 Total SVX4 current as a function of bias voltage with the maximum output driver current (id=7). The highest curve is for 2.75 V on the chip carrier, the middle curve is for 2.50 V and the lowest curve for 2.25 V. The horizontal scale is 10 μs /division, the vertical scale 50 mA/division, and the red line represents zero current.

9   Real Time Pedestal Subtraction

Many effects that contribute to noise (e.g. electromagnetic pick-up) influence all channels on a chip collectively as common mode noise. The SVX4 ADC is capable of performing a common mode (pedestal) subtraction. The subtraction of the pedestal in real time is also known as Dynamical Pedestal Subtraction (DPS). The circuitry for this is shown in Figure 17. For a more detailed study of the DPS circuitry in the SVX3 consult [6].
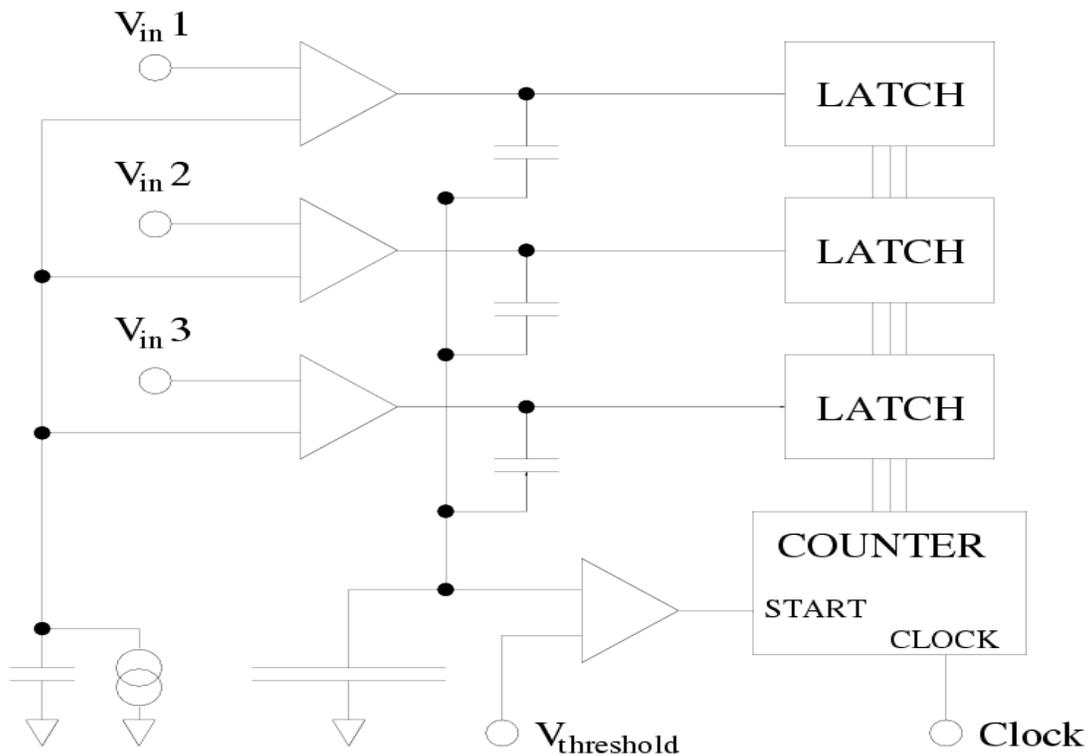
Figure 17 Cartoon schematic of the DPS circuitry inside the SVX4. As the ramp reaches the pedestal value for a particular channel, the comparator fires and increases the voltage on the DPS comparator shown in the middle of the figure. When the DPS comparator fires the clock begins to count, so if many channels are at pedestal the counter begins near the pedestal level.

In order to study the noise contribution with DPS on, the ADC has an analog delay built in so the baseline with DPS on is not at zero [7]. The threshold for the number of channels needed at pedestal in order for the DPS mode to operate properly is set using an external resistor. The DPS comparator has a 20 kΩ resistor to ground as a default, so the overall or equivalent resistance is calculated by computing the resistance of the default resistance with the external resistor on the hybrid. The equivalent resistance is used to bias a series of current mirrors inside the chip that effectively sets the threshold voltage. In Figure 18, we see the numbers of channels that are needed at pedestal as a function of the equivalent resistance in order for the DPS circuitry to operate properly.

Threshold versus R equivalent
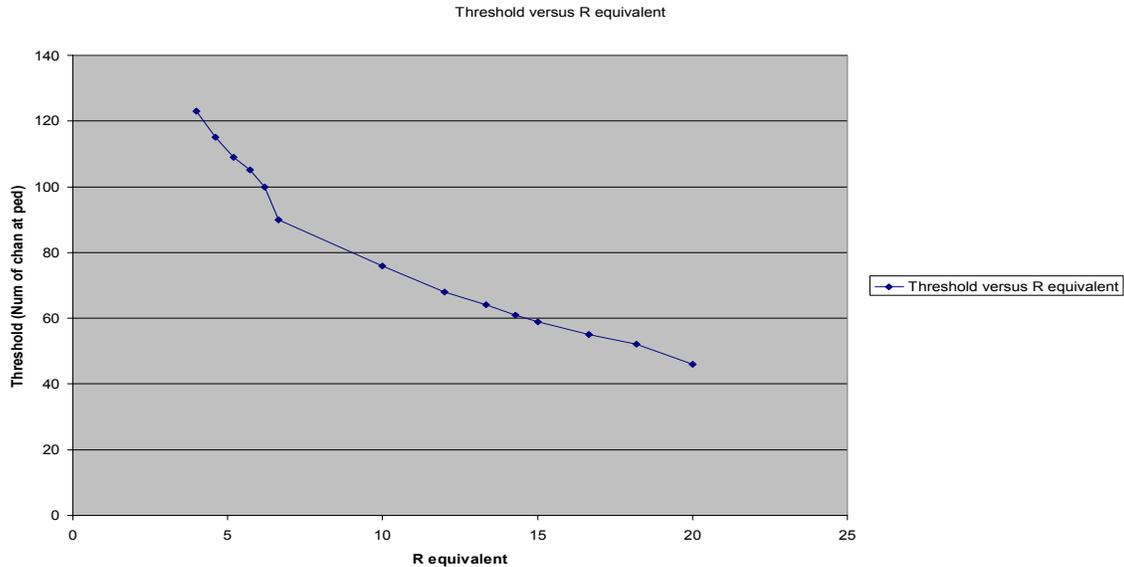
Figure 18 Number of channels needed at pedestal (DPS threshold) as a function of the equivalent resistance of the SVX4 chip with DPS on. With no external resistor, the default resistance is 20 kΩ and the DPS circuitry requires approximately 44 channels at pedestal.

In order to confirm that the DPS circuitry was working properly, we also measured the relative gain with DPS on and DPS off for a single channel of the chip as a function of the DPS threshold. In Figure 19, we see the relative gain for a single channel with DPS on and DPS off for a single channel with a 10 pF load. From the figure, it is clear the gain with DPS on and the gain with DPS off are similar.

In Figure 20, we see the analogous measurement of the relative noise between DPS on and DPS off. Again, the measurements are taken using the same channel with a 10 pF load. The graph clearly shows the noise with DPS on or off is similar.

Relative gain versus threshold
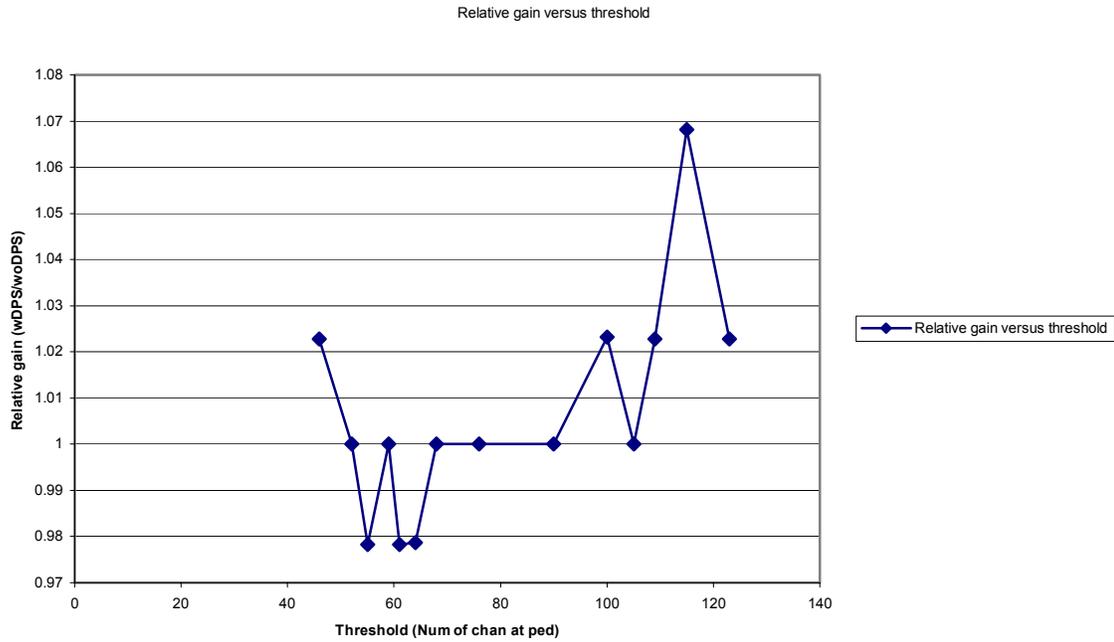
Figure 19 The relative gain of a bonded channel with a 10 pF load with DPS on compared to DPS off as a function of the DPS threshold.

Relative noise versus threshold
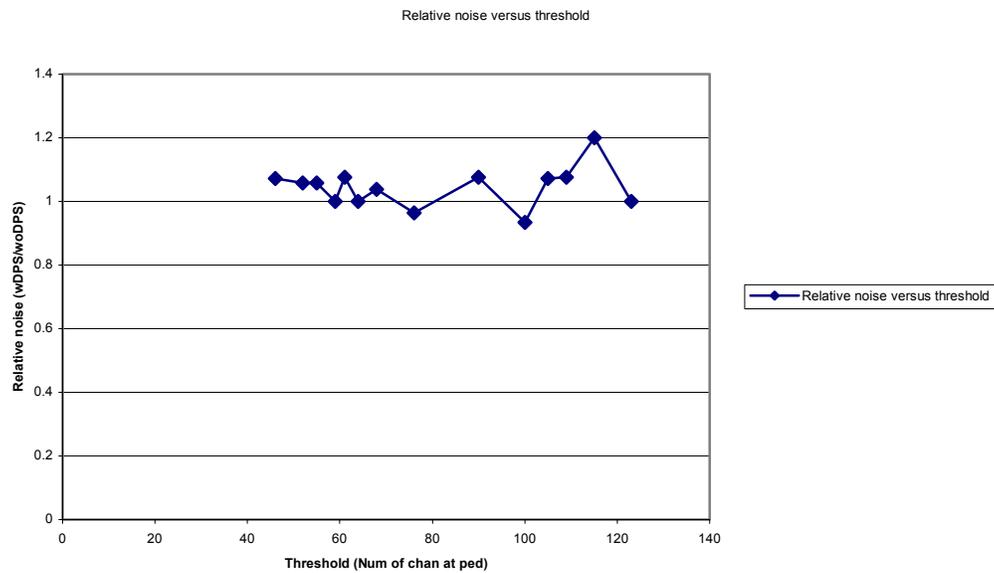
Figure 20 The relative noise of a bonded channel with a 10 pF load with DPS on compared to DPS off as a function of the DPS threshold.   It shows that with DPS on, no additional noise is introduced into the system.

10 Readout

Unlike the SVX4's precursors, the SVX4 does not use a collapsible output FIFO, but instead utilizes a token system. To confirm the functionality and to compare against simulation, we made the following measurements.

10.1 Output Driver and Current

We measured the output driver current of the data lines by placing scope probes on both sides of the differential bus line terminated by a 100 Ω resistor. By measuring the voltage on each side of the bus, the current can then be calculated. Table 7 shows the measured values as a function of the control bits downloaded to the chip.

Bit	Measured	Design
001	5.6 mA	5.6 mA
010	9.4 mA	9.2 mA
100	13.2 mA	13.4 mA

Table 7 Output currents for the data lines from the SVX4 chip as a function of the downloaded bits. The measured values agree well with the design values.

10.2 Double Readout

It is known from simulation that the readout of the SVX4 chip in sparse mode will produce a double readout of a single channel in certain conditions because of the token system. We are able to simulate the conditions for double readout using the following procedure. We set the readout clock frequency and then inject charge into the highest channel number. If we had a double readout, then we would inject on a lower channel number until the double readout disappeared. This way we could calculate the propagation time of the token (we know the clock frequency) and then predict where the double readout would occur for different readout clock frequencies. This worked very well. In Figure 21, we show the threshold for double readout as a function of the readout frequency. A clear linear relationship is observed. As the readout frequency gets higher, the threshold for double readout is lowered.

**Double Readout as a Function of Frequency**
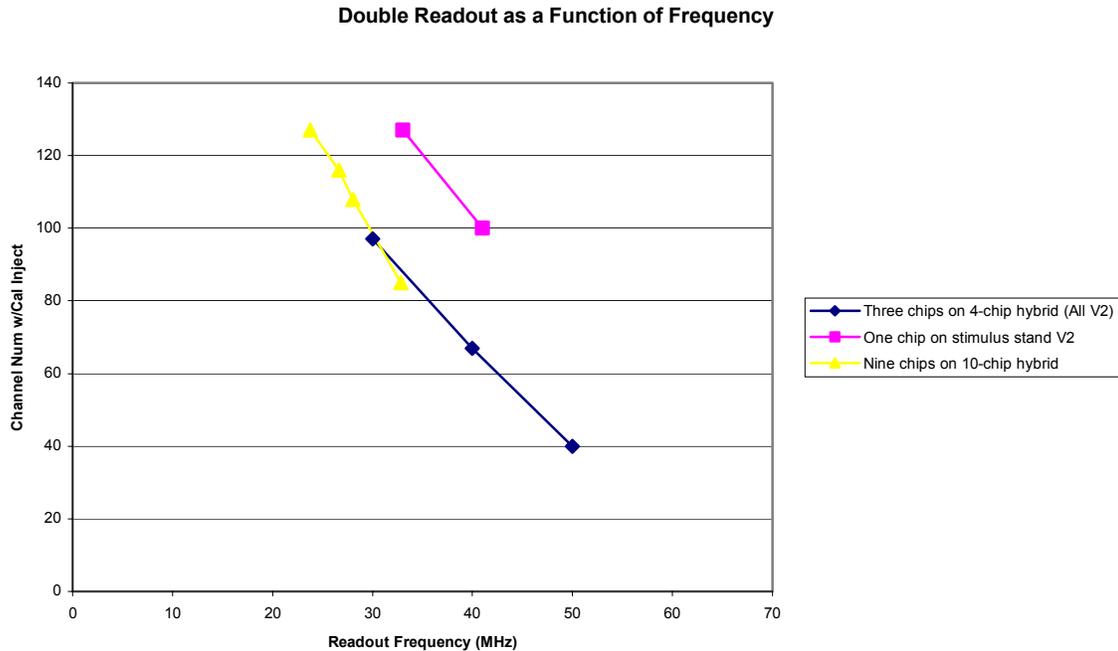
Figure 21 Threshold for double readout as a function of the readout frequency clock. For example, for three chips on the four chip hybrid, setting the readout clock frequency to 40 MHz will give a double readout if the charge is injected on channel 62.

It was found that no double readout occurred for the first chip on the four or ten chip hybrid during this procedure. Through further investigation, a double readout could be produced if the time between the signal Priority In going low and the first back end clock pulse was less than one-half the readout clock frequency. This is shown in Figure 22. If the time between Priority In and the first back end clock was less than 19 ns, a double readout of the first chip occurred.

We also conducted a study to observe how the threshold for double readout depended on the DVDD voltage supply. From simulation we know that the speed of the token is increased as the DVDD voltage supply is increased. In Figure 23, we show how the threshold for double readout increases linearly with increasing DVDD voltage. We used four different chips on individual chip carriers for this study. It is important to note that the frequencies for producing a double readout on chip carriers are higher than normal because the signal PriIn is programmed to go low at a certain time in the readout cycle on the Stimulus Test Stand. Only when the frequency of the readout clock is at a high enough frequency does the timing correspond to one half the clock period as seen with the D∅ hybrids, then the double readout occurs. That is acceptable because our measurement was aimed to study double readout as a function of DVDD and it is seen to be linear as expected.
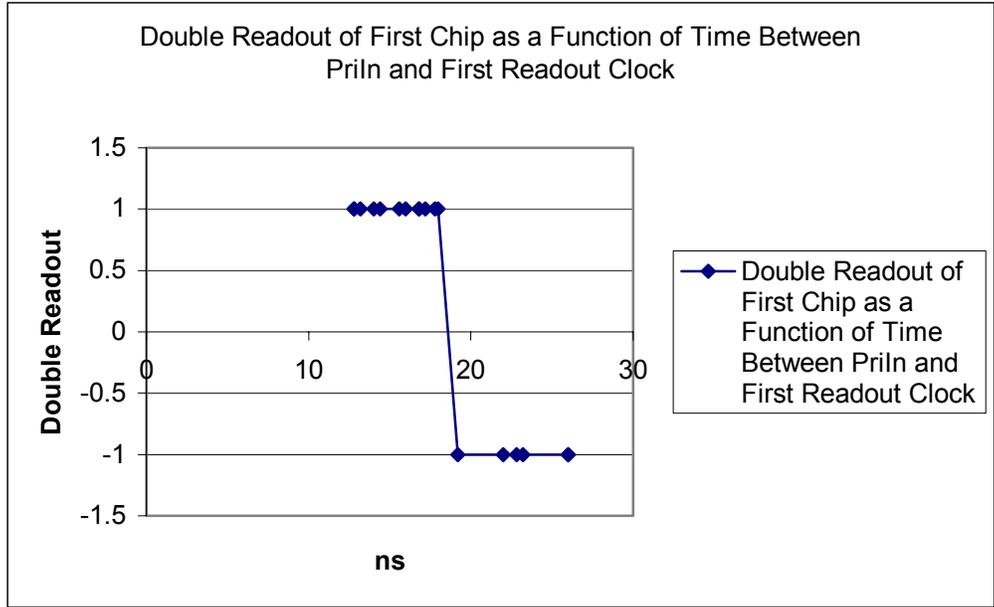
Figure 22 Double readout of the first chip of the ten chip hybrid as a function of the time between Priority In going low and the first readout clock edge going hi.   The value 1 is used in a Boolean fashion. This means a double readout occurs when the value is 1 and the double readout does not occur when the value is –1. The transition occurs at approximately at 19 ns which is one-half of a clock cycle at 26.5 MHz.
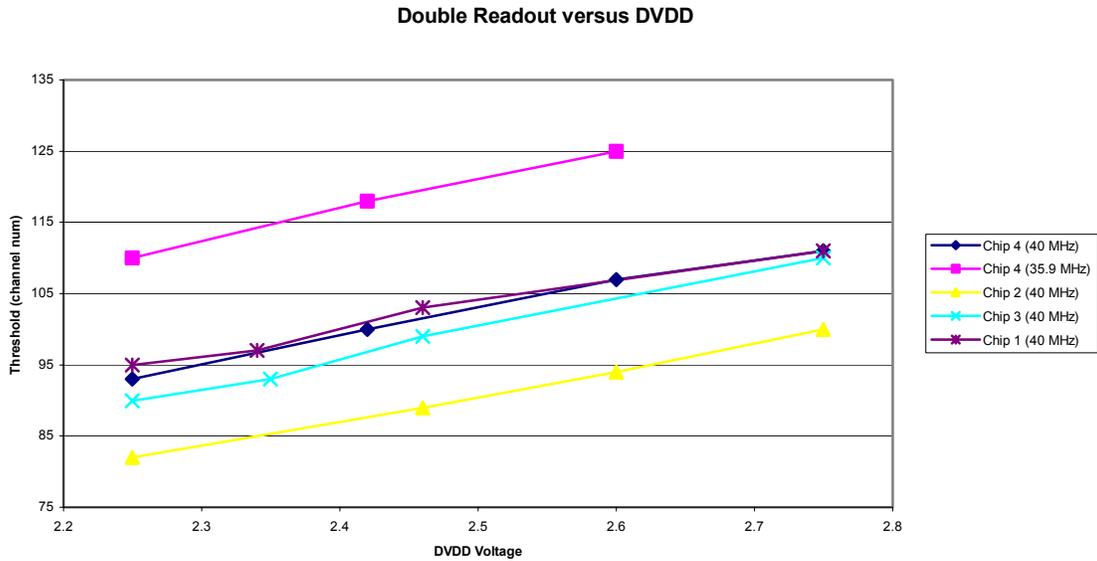
Figure 23 Threshold of double readout as a function of DVDD. It is clear from the figure that as DVDD is increased, the threshold for double readout increased because the speed of the token is increased. These results were obtained using four different single chip carriers at higher than normal back end clock frequencies.

We also studied the double readout using different configurations of the charge injection mask. In Table 8, we show the data output from an SVX4 chip when the double readout conditions are satisfied. In the far left column of the table, only one channel has charge injected into it, e.g. channel 71 (hex). It should be noted that the sparsification feature of the chip is turned on and the threshold for readout is placed high enough to ensure only those channels with charge injection will be readout. The second column shows that if multiple channels are injected on – channels 7d (hex) and 7e (hex), then only the first channel of the pair gives the double readout. The third column confirms that if the charge injected channel (e.g. channel 0 (hex)) – can be reached by the token before two back end clock cycles occur, no double readout occurs. Other columns are obvious, but the last column shows the Read Channel 63 feature of the chip prevents double readout from occurring.

Channel Output	Channel Output	Channel Output	Channel Output	Channel Output	Channel Output	Channel Output
71	7d	00	00	00	00	00
71	7d		7f	7e	01	01
	7e		7f	7e	7e	3f
				7f	7e	7e
					7f	7f

Table 8 Output from the SVX4 showing the double readout for various configurations of charge injection masks. A channel in the readout means that the channel had charge injected on it and the ADC value was above the digital threshold with data sparsification on. The final column shows that turning on the feature to Read Channel 63 all the time prevents the double readout from occurring.

10.3 Additional Readout Features

The SVX4 has additional readout features whose functionality was confirmed by all test stands. For example, the Read All feature was confirmed with DPS on and DPS off. The Read Neighbor bit was confirmed to work as well. Read Channel 1, Read Channel 63, and Read Channel 128 were all confirmed to be functional. These features were added for different reasons. Counter Modulo and the Digital Threshold were also confirmed to be functional.

10.4 Frequency Margin

In experimental conditions, it is impossible to transmit a perfect clock to the components of the system due to transmission through long cables. So, the chip must be able to function or be able to readout if the back end clock does not have the optimum frequency (f = 25.6 MHz) or 50% duty cycle. We tested this ability by varying the frequency and duty cycle of the back end clock during digitization and readout.

Worst case conditions require that the chip operate within a 20% frequency margin and a 40/60 -60/40 duty cycle. We have confirmed that the chip works within the required frequency margin and duty cycle for both digitization and readout. At each frequency and duty cycle, a pedestal run was taken along with a calibration injection on every tenth

channel to confirm proper operation of the chip. In addition, we found that we could increase the speed of readout up to 50 MHz and the chip would function properly [8].

11 Black Holes (Pinholes)

In the silicon detector, the AC coupling capacitor that connects the biased silicon strips to the input of the preamplifier of the chip can be damaged or destroyed. This causes a large amount of current to flow into the preamplifier completely saturating the input of the channel. Because of such a large current flow and the input of the amplifier being forced to ground, it becomes possible to forward bias the diode structure between the input channel and substrate of the chip forming a weak n-p-n transitor with a neighboring channel. Therefore, the input channel with the shorted capacitor shares charge with the neighboring channels. In Figure 24, we see a cartoon schematic showing a shorted coupling capacitor and charge sharing through the substrate.
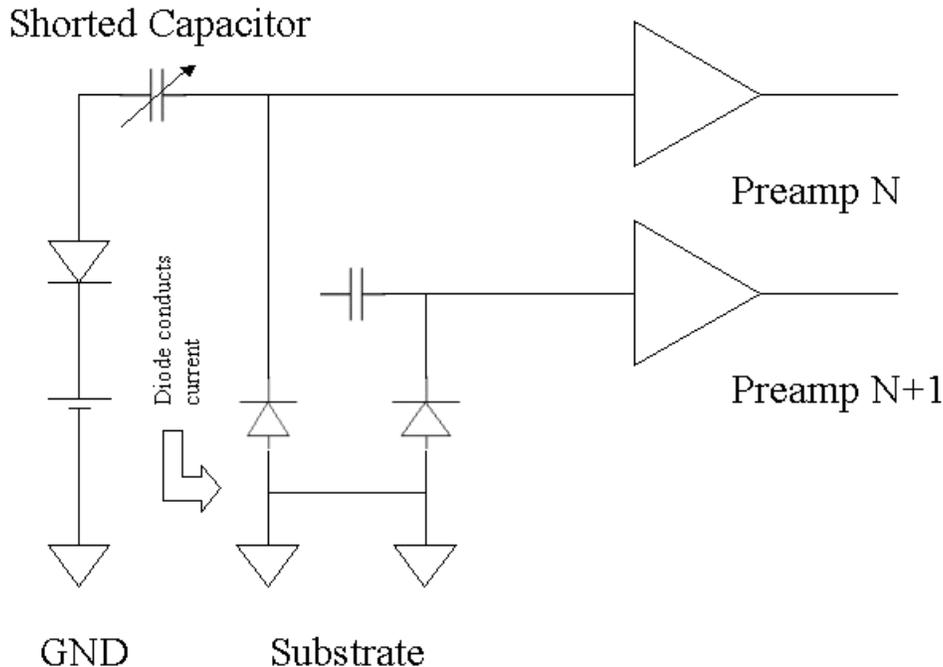
Figure 24 Cartoon schematic showing the charge sharing between neighboring channels when a pinhole exists on the silicon sensor.

When such a situation occurs, the pedestal saturates and the noise drops to zero with the neighboring channels incurring higher noise. There is no way to disconnect the channel with the shorted capacitor once the detector is installed. Therefore, the input from the channel with the pinhole and the neighbor channels must be discarded resulting in a loss of fiducial coverage and additional noise introduced into the system. If one looks at the noise as a function of channel number, one sees the noisy channels around the pinhole and a zero value for the channel with the pinhole. This looks very similar to a space-time diagram of a black hole and therefore the name was adopted.

The SVX4 has a new feature which allows the channel with the black hole to be disconnected so that neighboring channels are unaffected by the large draw of current. In the downloaded bit stream, a bit controls whether the channel mask is used as a charge injection mask or a mask against black holes. Essentially, when the mask is used to disconnect pinholes, it forces the preamp reset for the channel to be engaged during data taking and it is able to source the current from the damaged capacitor reducing the noise.

To simulate a black hole and confirm the new feature of the chip works properly, we did a study using a current source connected directly to the input of the channel (with no coupling capacitor). We increased the current in a linear fashion. We sourced up to 3.5 mA and saw no charge sharing at all between neighboring channels without the black hole mask active. We have also confirmed that the black hole fix works by injecting a square pulse into the channel and seeing no response with the black hole mask active. We investigated any possible unknown systematic effects by sinking up to 3.5 mA as well. In conclusion, it appears that the channels are robust enough not to be affected by a pinhole.

12 Voltage Supply Issues

We investigated the ability of the SVX4 chip to survive over voltaging without incurring damage. For this study, we combined the two power supplies to the chip (AVDD and DVDD) into one power supply to simplify the procedure. The test consisted of setting the power supply voltage to a set value and then taking a data cycle with the test stand [9]. If the power supply voltage was outside the specifications (2.25-2.75V for both AVDD+DVDD), then after that data run the voltage supply was brought back to 2.75V and a new data cycle was taken and compared to previous data runs. This was done to confirm the proper operation of the chip and to confirm no damage to the SVX4 had occurred.

The point of this test is to explore the voltage ranges that the SVX4 can handle without being permanently damaged. The results were as follows: After 6.8V, we vaporized a wire bond connected to DVDD because the current draw was greater than 1A. From this we conclude that it is more likely overvoltages will vaporize a wire bond instead of damaging or destroying the SVX4 chip in the experiment. Another feature of the SVX4 that was investigated was the possibility of latch up when turning on the power supplies to the chip. The SVX2 has a controlled sequence of how the power is applied to the chip to prevent such a situation from occurring. Since the Stimulus Test Stand has manually controlled power supplies, we randomly turned on the supplies for AVDD and DVDD. We also randomly lowered and raised the power supplies and could not produce any latch up behavior as observed with the SVX2. It is important to note that if the voltages were taken outside the specifications of the chip, it was sometimes necessary to reinitialize the chip to get proper behavior, but no latch up behavior was observed.

13 Differential Non-linearity Studies

These studies were done using the full chain test stand for Run IIb located at D∅ DAB. The test stand consisted of connecting an external voltage to the calibration injection circuitry. The voltage waveform was set to a sine wave with a very low frequency (1

kHz). This is much slower than the data sampling rate of the SVX4 – which depends on the front end clock frequency and duty cycle.

The idea consists of scanning or supplying all possible voltages to the inputs of the chip in order to study effects in the ADC. The specific effect that this study is searching for is called the differential non-linearity. In simple terms, a perfect ADC will increment the binary counter for every equal increment of voltage or charge, but it is possible that the conversion from the state 0 to state 1 of the least significant bit requires a different amount of charge as compared to the conversion from state 1 to state 0.

To measure this effect we show the result of the experimental setup in Figure 25. In order to make a quantitative measure we must exclude the edge regions because these regions measure the peaks and valleys of the sine wave and we are only interested in the linear region. Using the middle region of the histogram, we sum the number of contributions from odd ADC values (transitions from state 0 to state 1), sum the number of contributions from the even ADC values (transitions from state 1 to state 0), and then sum all contributions in the middle region. The differential non-linearity, DNL, is then calculated from

$$DNL = | \Sigma_{even} - \Sigma_{odd} | / (\Sigma_{even} + \Sigma_{odd}) \times 100\%$$

A large value of the DNL means that it takes a different amount of charge to flip the LSB of the ADC from 0 to 1 than from 1 to 0. Due to the design of the calibration circuitry, the hybrids are unable to source a completely linear voltage for all chips in the D∅ hybrid, so we were not able to calculate a reliable value for the DNL, but LBL used the PATT board test stand with a single chip and calculated a value of 5%. The Stimulus Test Stand is presently unable to make this measure, but will in the near future.
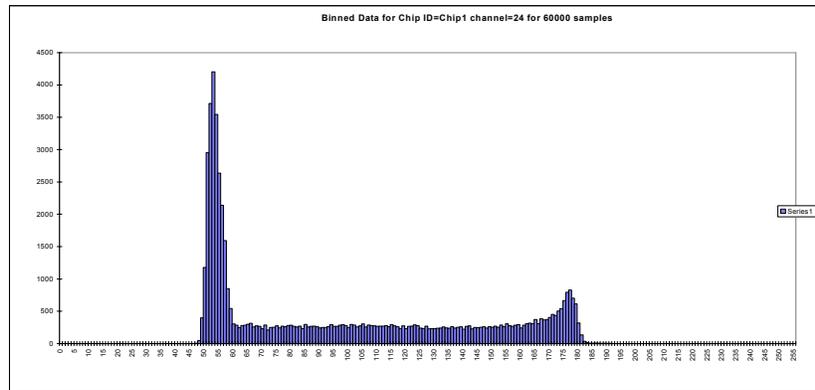
**Figure 25 Differential non-linearity (DNL) for a ten chip hybrid. The offset is because of the analog delay in the ADC from the DPS circuitry. The plot is not symmetrical due to the voltage divider effect on the calibration input from the 10 chips on the hybrid which does not allow an exact measurement on the DNL with the full test chain readout. This will be corrected in the next version of the chip.**

14 Data Persistence

We also investigated the data persistence using the D∅ hybrids with the full D∅ test chain. The object of this measurement is to see if the resistance of the MOSFET transistors used to switch in and out a capacitor in the pipeline have a high enough resistance relative to the substrate to prevent substantial leakage of charge out of the pipeline capacitor. If not, the leakage of charge of the cell would introduce an error into the measurement. We show a cartoon picture of a single pipeline cell in Figure 26.


Data persistence, $\tau = RC$
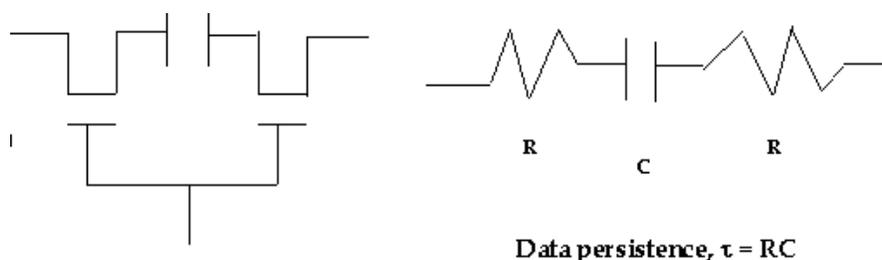
Figure 26 Cartoon schematic of a pipeline cell in the SVX4. The left picture shows how two FETs surround a simple capacitor. The FETs operate as simple switches and allow charge to flow when the clock signal is high. When the clock signal is low the FETs act as large resistors which prevent the leakage of charge from the pipeline cell.

By measuring the time of the persistence of the data, one can estimate the resistance of the FET transistors. The value of the capacitance of the pipeline cells is C=10 pF. Using the D∅ test stand, we acquired an event and waited longer and longer times before reading out the data. We observed a shift in the baseline of the pedestal for time longer than 1 ms which indeed demonstrates the FETs have a large resistance that prevents charge leakage.

15 Electrostatic Discharge Testing (ESD)

It is important to measure the ability of the chip to resist damage from an electrostatic discharge and to test the ESD protection circuitry. In Figure 27, we show the experimental setup that was used to simulate an ESD using the human body model. The human body model consists of a 680 pF capacitor and 1.50 kΩ. In Figure 28 and Figure 29, we show the output waveform from the test setup in a standard and expanded view, respectively.

01/26/2001

ESD Test Setup Schematic

HP 4145B Semiconductor Parameter Analyzer

ESD Test Board

40 Pin ZIF Socket

HV Power Supply

HV Resistor Box

0 - 10 KV

500M ohms

100pf Cable Cap.

1.50K ohms

39 ohms

680 pf

HV Reed Relay

Coto 5501-12-1

+12V
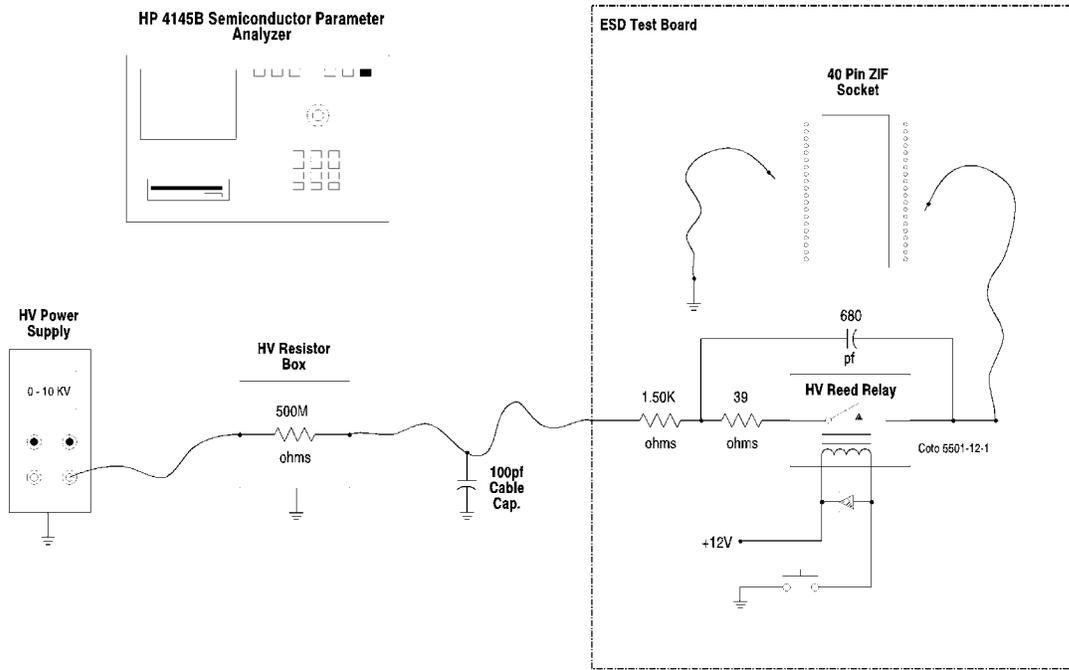
Figure 27 ESD test setup showing the use of the human body model.

The procedure consisted of testing the control lines first by increasing the voltage of the ESD pulse. The ground return used on the chip was an analog ground located directly next to the chip on the SVX4 chip carrier. A single control line (BE_CLK) was subjected to increasing ESD pulses increasing from 100-500V in 100V increments, then in larger steps of 1000V increments. The control line was found to be resistant up to 6000V and was not damaged. An input to the SVX4 chip was also subjected to ESD pulses in the same manner as the control line. Again, the inputs were resistant up to 5000V, but incurred damaged at 6000V. The channel did not respond to calibration injections after this procedure. This means that the chip is very resistant to damage from ESD pulses.
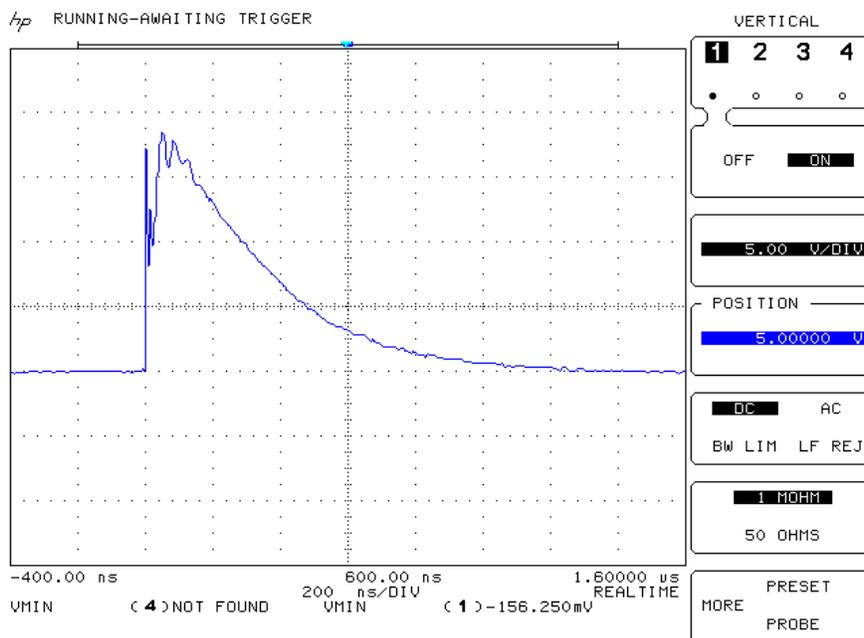
**Figure 28 The output waveform from the ESD setup. The horizontal scale is 200 ns/div and the vertical scale is 5 V/div.**
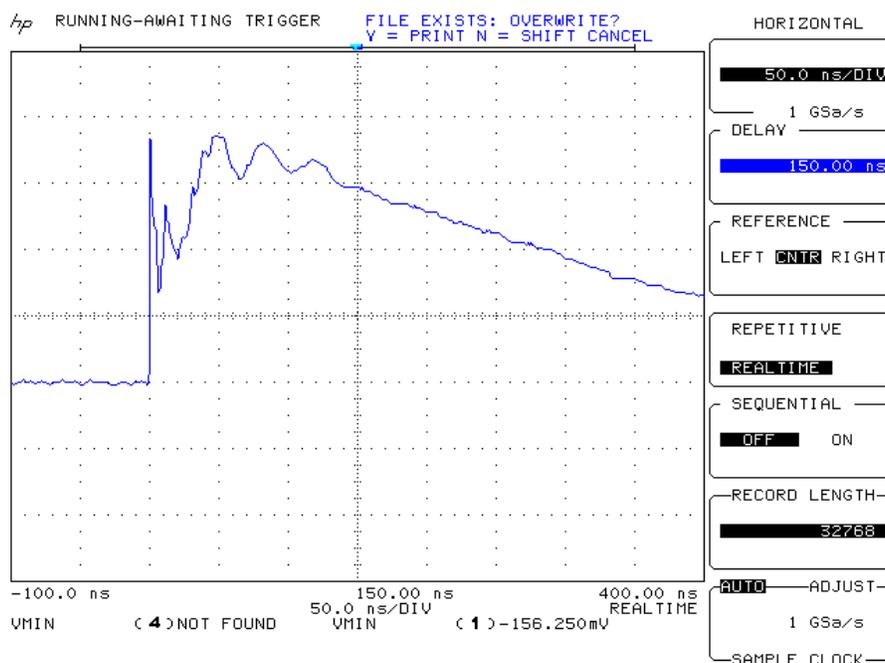
Figure 29 A magnified view of the output waveform from the ESD test setup. The horizontal scale is 50.0 ns/div and the vertical scale is 5 V/div.

16 Performance Issues

The current SVX4 design currently has three problematic issues: pedestal nonlinearity, channel to channel variations outside the design specifications, and a pipeline nonlinearity. In the following sections we will explain these problems and describe in more detail the studies that have been done.

16.1 Pedestal Nonlinearity

It was discovered that certain operating parameters produce a nonuniform pedestal distribution. This is problematic because in sparsification mode, only a single digital threshold can be set and therefore different channels will have different efficiencies for being readout. In Figure 30, we show the pedestals for all 128 channels in an operating range where the nonlinearity or bow is present.
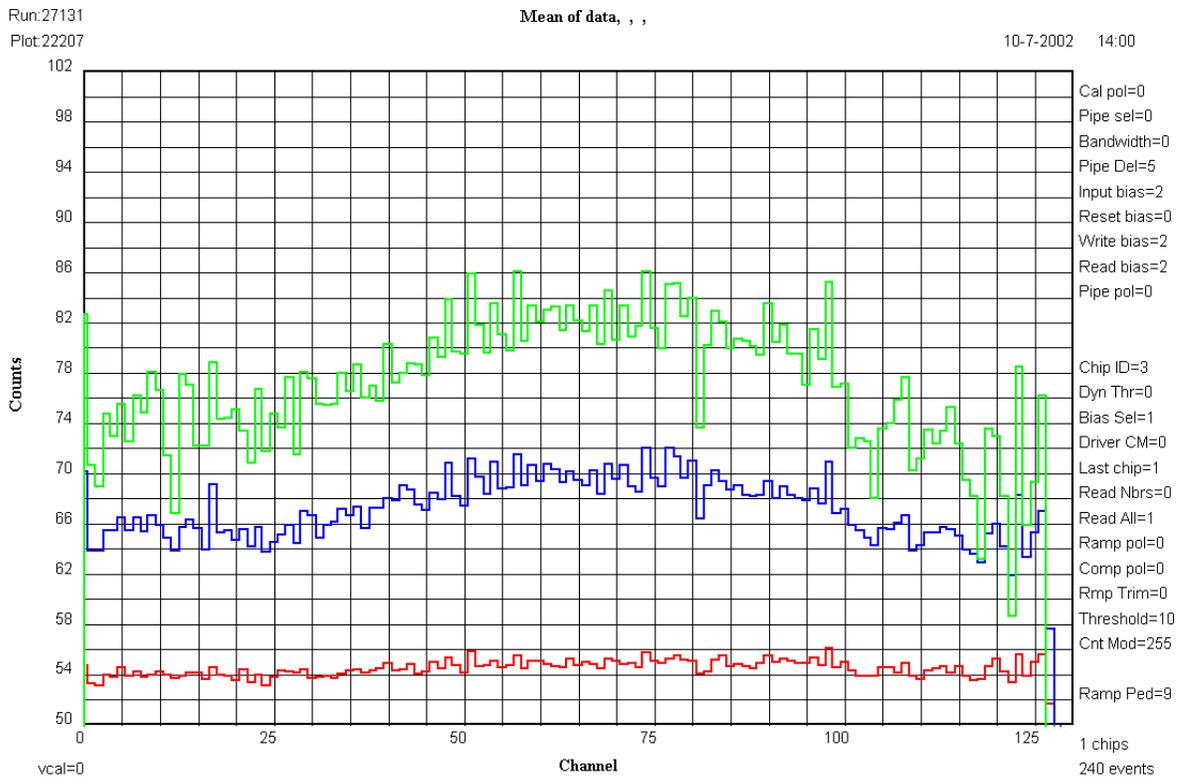
Figure 30 The bowing as a function of the I quiescent current of the chip. As the I quiescent current is increased the bowing decreases. This is because the larger the I quiescent value the faster the comparators become decreasing the time difference between adjacent channels. The green line corresponds to V=510 mV (I=153μA), the blue line corresponds to V=530 mV (I=190μA), and the red line corresponds to V=610 mV (I=398 μA).

The pedestal bowing is conjectured to be coming from the slew time of the comparators. By increasing the I quiescent current, we were able to reduce the nonlinearity to an acceptable level as shown in Figure 30. In Figure 31, we give a cartoon description of how different slew times in neighboring comparators produces a nonlinearity in the pedestal. This figure also shows how channel to channel variations can be quite large in the chip which will be discussed in the next section.
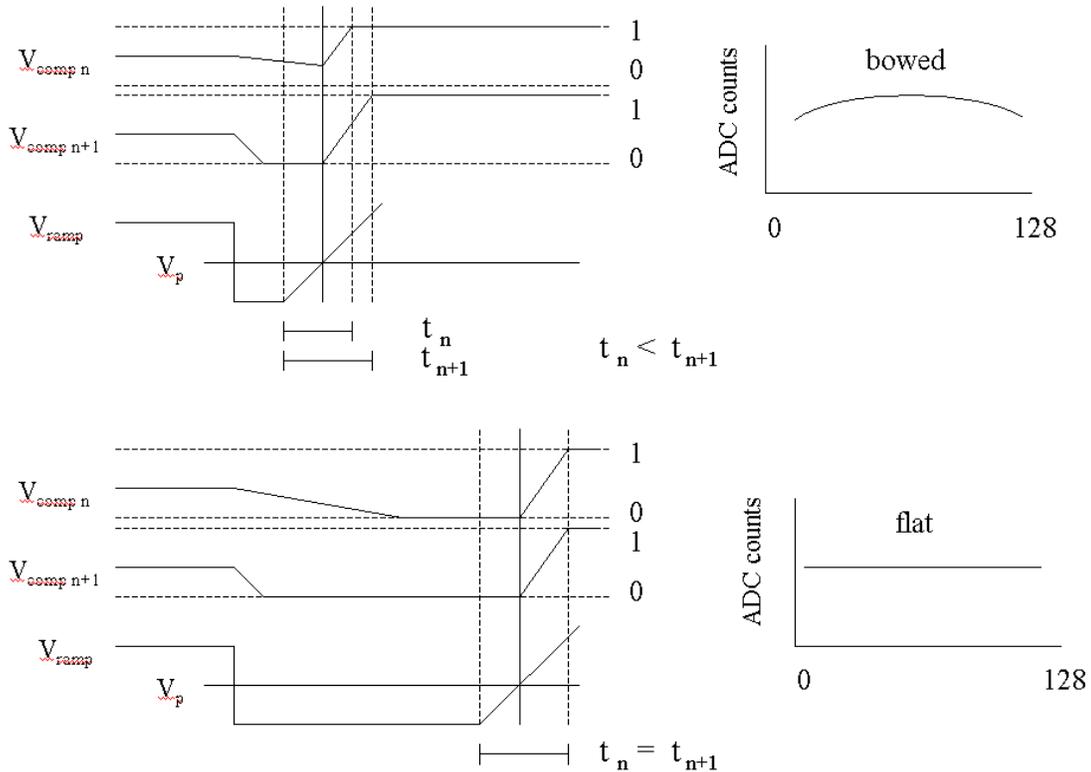
Figure 31 Cartoon showing how the nonlinearity in the pedestals can occur in the SVX4 and how the channel to channel variations happen due to the slew time or speed of the comparators. If the slew time in the comparator for channel n is longer than the slew time for channel n+1, then during digitization the slower comparator (n) does not attain its proper operating value and will reach the logical level 1 before the comparator with the proper slew time (n+1) does, therefore creating the nonlinearity in the pedestal.

This explanation can also be confirmed by allowing more time for the comparators to settle before releasing the ramp used in digitization and then observing the pedestal structure. This study can be seen in Figure 32. In this study, the time interval between releasing the comparator reset signal, which activates the comparators, and the releasing of the ramp reset signal was linearly increased by a front end clock cycle until the nonlinearity disappeared in the pedestal distribution.
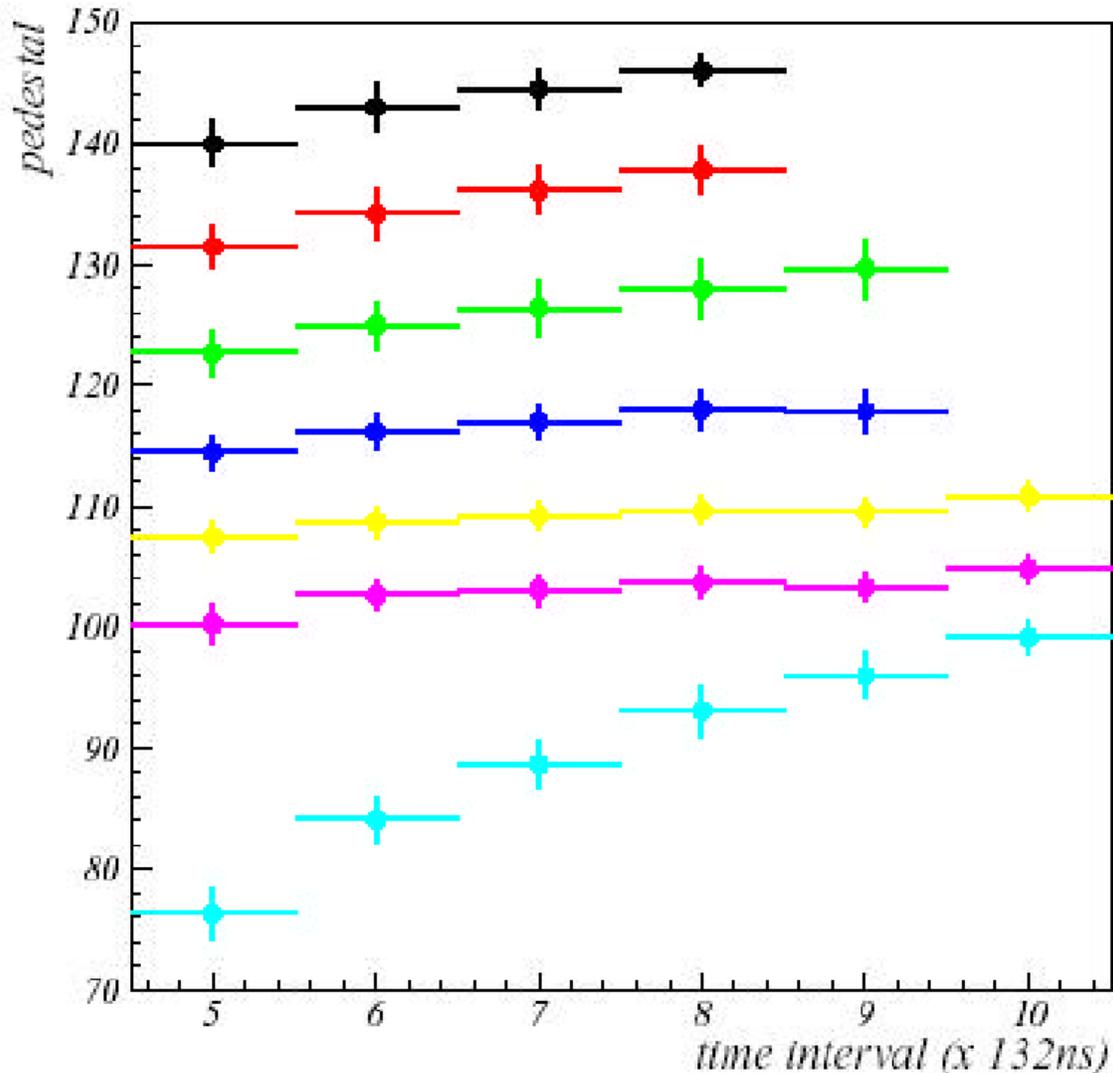
Figure 32 Histogram showing the average pedestal value as a function of the time interval between comparator reset and ramp reset. As the time interval is increased the average pedestal value attains a constant value which means that the pedestal is uniform. This graph also shows that the higher the pedestal values the lower the nonuniformity because it takes a longer time for the ramp to reach these higher values and therefore the comparators have a longer time to settle before the need to change state.

16.2 Channel to Channel Variations

Similar to the discussion in Section 16.1, if the channel to channel variation are large then each channel will have a different efficiency for readout with sparsification on. It is also believed that the channel to channel variations are from the slew times of the comparators. We can test this hypothesis by increasing I quiescent. By increasing I quiescent the slew time of the comparators should significantly decrease and the channel to channel variations should disappear. In Figure 33, we show the effect on the channel to channel variations as a function of increasing I quiescent. Notice that the high pedestal values with the larger channel to channel variations correspond to lower I quiescent

values. As I quiescent is increased, the channel to channel variations are decreased as expected.
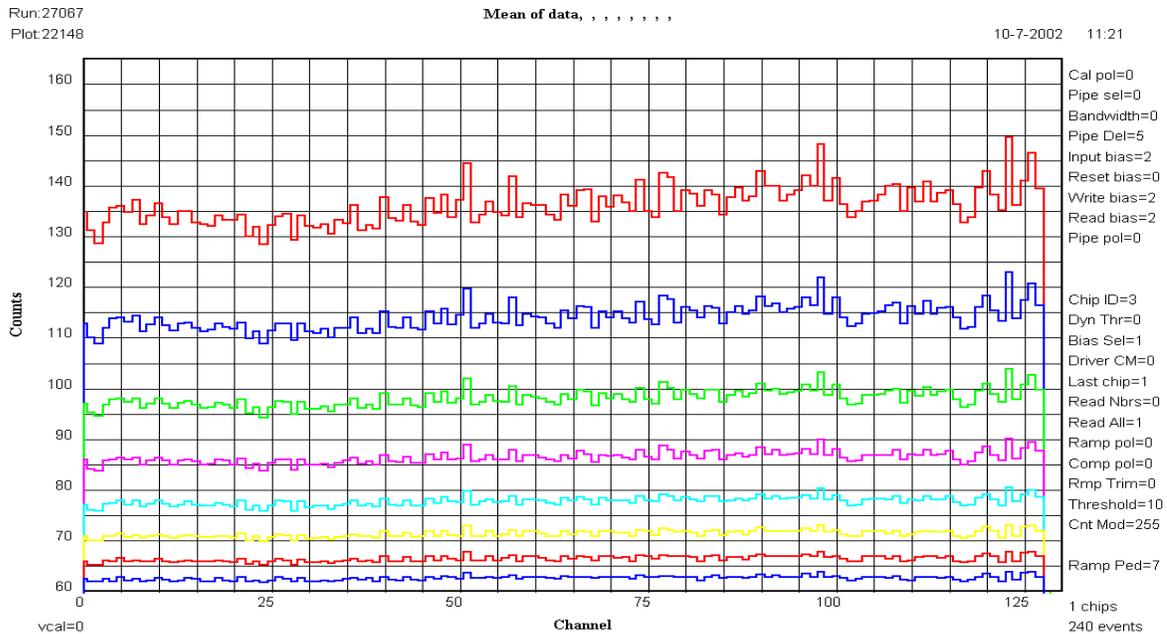
**Figure 33 Channel to channel variations as a function of the I quiescent current to the chip for ramp up values only. The data in the plot are as follows: red line, V=490 mV, pedestal = 135, I slope= 117 μA; blue line, V=510 mV, pedestal = 112, I slope= 153 μA; green line, V=530 mV, I slope= 190 μA; maroon line, V=550 mV, I slope= 235 μA; light blue line,V=570 mV, I slope= 294 μA; yellow line, V=590 mV, I slope= 337 μA; red line, V=610 mV, pedestal = 65, I slope= 398 μA; blue line, V=630 mV, pedestal = 62, I slope= 461μA.**

16.3 Pipeline Nonlinearity

It was also discovered that the pedestal systematically increases as a function of the pipeline cell number. Currently, it is not understood why this effect is present, but the leading explanation is that a considerable resistance has developed along the traces connecting all the capacitors in the pipeline inside the chip. As one progresses up the pipeline the resistance keeps getting larger and larger and therefore it changes the amount of charge deposition on the capacitor in the pipeline. In Figure 34, we show the average pedestal value as a function of the pipeline cell. It is clear the higher pipeline cell numbers give higher pedestal values. In Figure 35, we show two fits (linear and polynomial) to the data. It is clear from the R value that the dependence of the pedestal on pipeline cell number is linear.
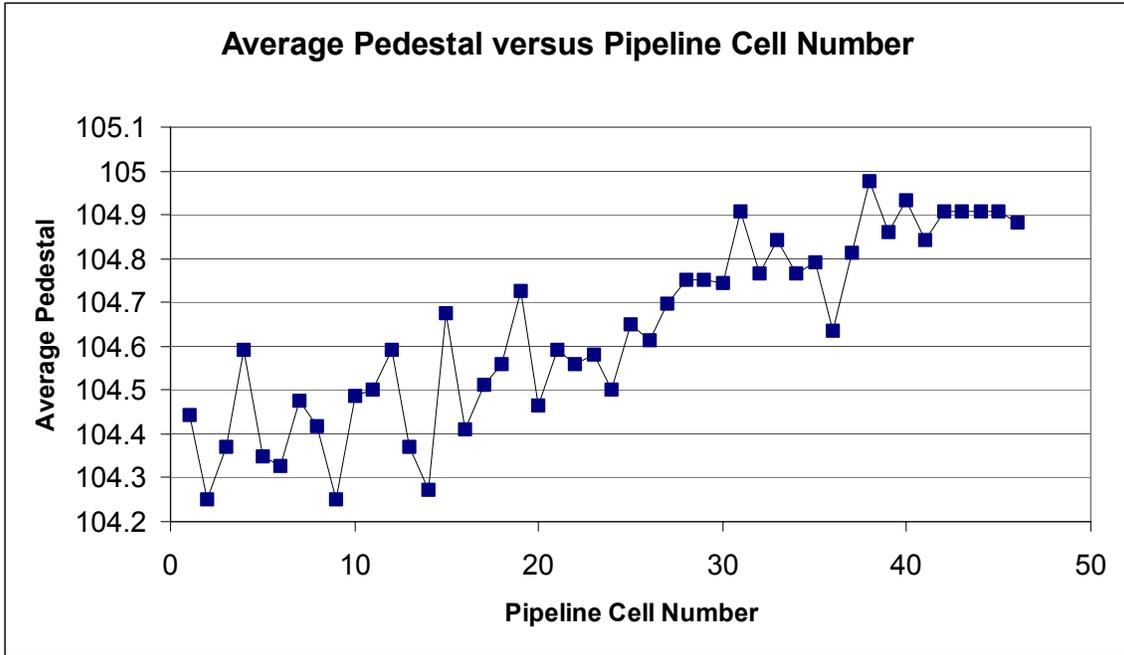
Figure 34 Average pedestal as a function of the pipeline cell number for an individual channel. The channel number used in the figure was number 63.
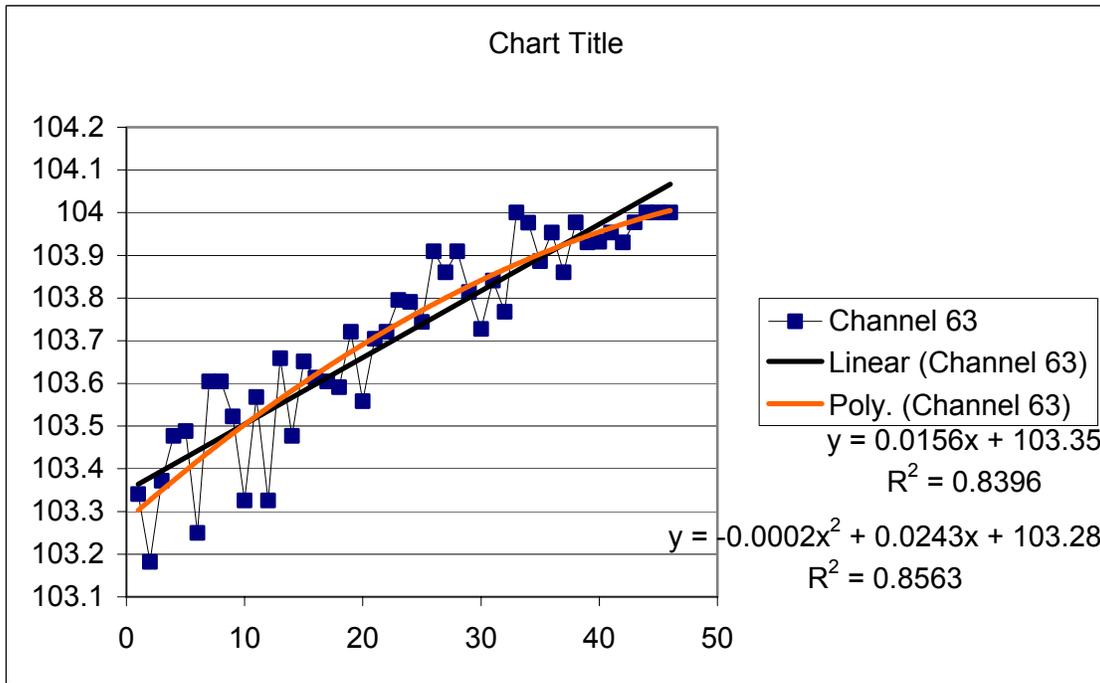
Figure 35 Linear and polynomial fits to the nonlinearity in the pipeline. The R value from the linear fit is smaller which shows the dependence in linear.

We also carried out an exhausted study of the slope of the pipeline as a function of channel number to investigate if the nonlinearity was related to the bulk geometry of the chip. In Figure 36, we show the pipeline nonuniformity for three different channels.

These channels were chosen because channel 1 and 126 occur near the edges of the chip and channel 63 is in the middle of the chip.
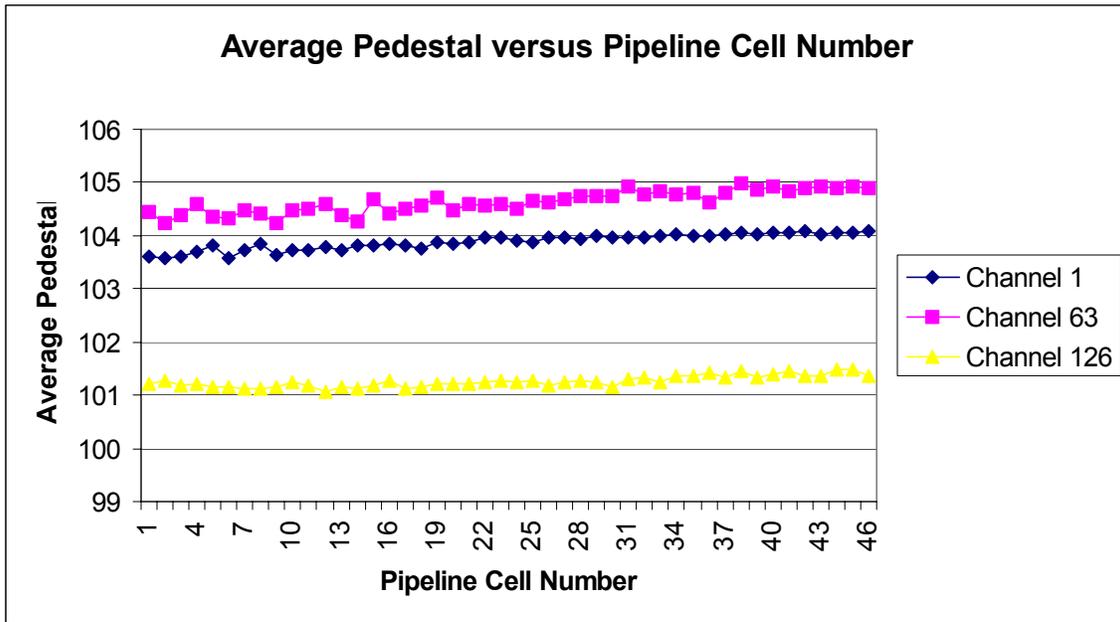
Figure 36 Comparison of the pipeline pedestals from different pipelines cells for different channel numbers.

If Figure 37 we see a three dimensional plots that shows the nonlinearity of the pipeline as a function of the channel number for the entire chip.
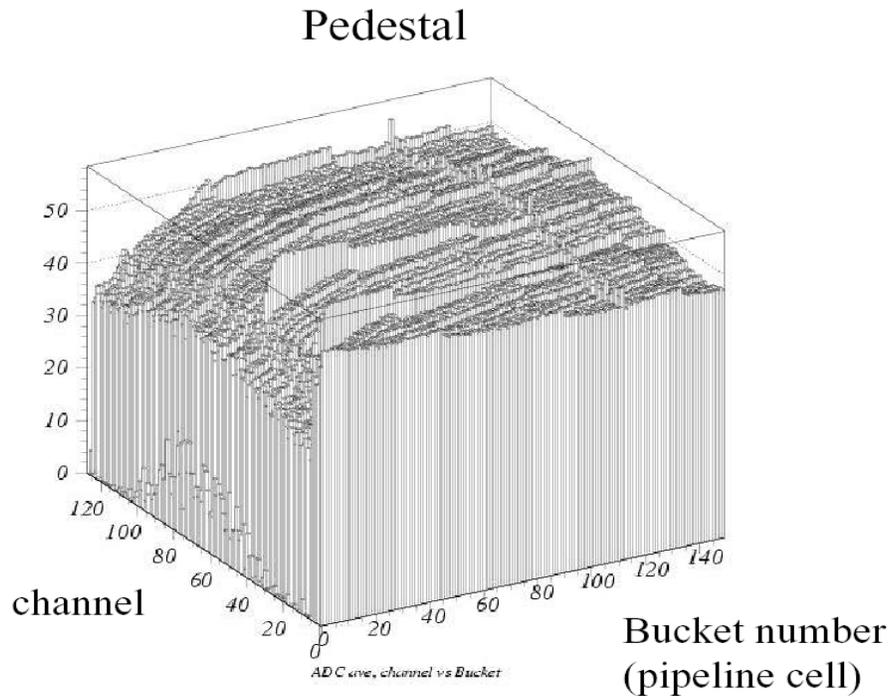
Figure 37 Three dimensional plot showing the nonlinearity in the pipeline for all 128 channels of the chip.

We also confirmed that the nonuniformity was not coming from a coupling between the analog and digital sections of the chip. In order to confirm this we turned on the preamp reset throughout the acquire cycle and observed the pedestals. We show the results of this study in Figure 38. It is clear from this plot that the nonlinearity in the pipeline remains even though the pipeline reset is held high and no data can be taken. We did exhaustive voltage supply studies and found a slight dependence on AVDD, DVDD, and the relative difference between AVDD and DVDD, but nothing that would demonstrate a conclusive reason for the nonlinearity.

Average Pedestal versus Pipeline Cell Number
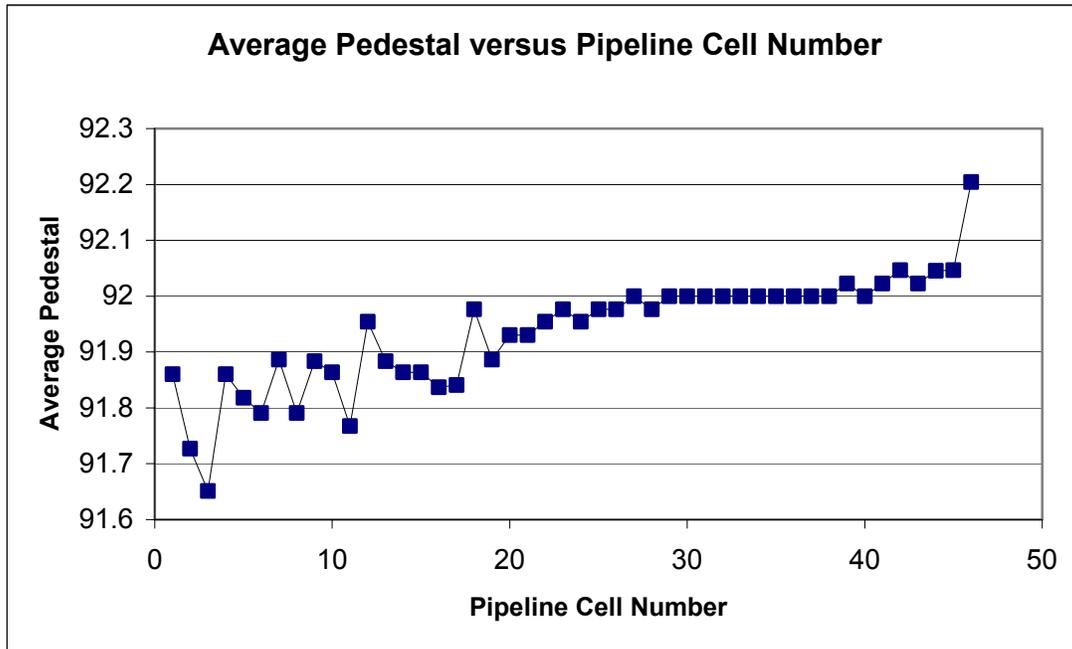
Figure 38 Average pedestal versus pipeline cell number. The data was taken with the preamp reset held high through out the acquire data cycle. The data for this plot is from channel 63.

16.4 Receiver Failure

It was observed that high I quiescent current values or small I quiescent values affected the proper operation of the chip. The reason was found to be improper sizing of the transistors in the receiver layout portion of the chip. In Figure 39, we see the DVDD current consumption as a function of the I quiescent current.
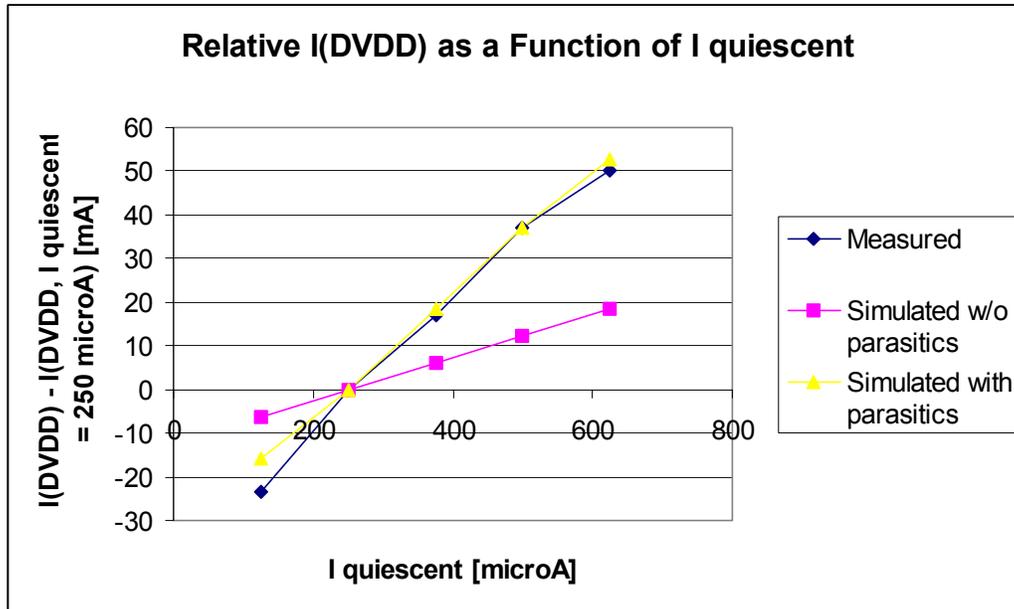
Figure 39 Relative current consumption of DVDD as a function of the I quiescent current from measurements and simulation.

17 Radiation Hardness of the SVX4

The shift register and the shadow register in the SVX4 are a new design, so it is necessary to confirm the radiation hardness of the design. The is very important because a charged particle may flip a bit in the shadow register which would change the operating parameters during data taking. SEU and irradiation studies of the SVX4 chip were done at the University of California Davis and the Kansas State University [10] and are only summarized below.

17.1 Single Event Upsets

The shift register and the shadow register of the SVX4 are basically memory cells. In Figure 40, we show a schematic of a CMOS memory cell. In Figure 41, we see the CMOS memory cell drawn with its component transistors. If a charge particle passes through a transistor, it could deposit or extract enough charge to turn on or turn off the transistor, respectively, which then would change the value of the memory cell and therefore the operating parameter of the chip. This is called a Single Event Upset.
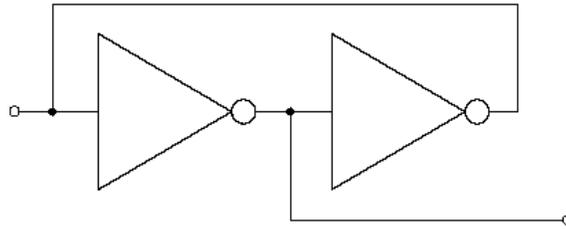
Figure 40 Cartoon picture of a CMOS memory cell. This is a basic picture of one of the cells in the shadow register.
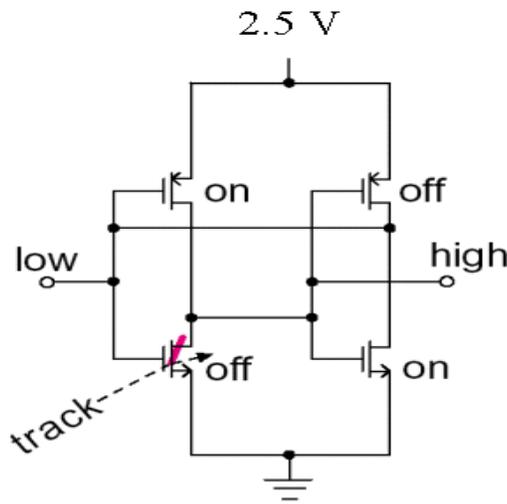
Figure 41 Cartoon schematic showing how a highly ionizing particle can flip a CMOS transistor from the off state to an on state creating a SEU.

In order to detect an SEU, certain parameters of the chip were set and then the chip was constantly read out to confirm the data corresponded to the downloaded operating parameters. If the values read out did not correspond to those values downloaded, an SEU occurred. For example, the counter modulo would be set below the pedestal value and the data readout for each channel should correspond to the counter modulo. If a different value was readout than an SEU occurred with one of the bits in the counter modulo bit field.

The SEU tests at the UC Davis cyclotron were done with 63 MeV protons at fluences up to 1.4E14 $cm^{-2}s^{-1}$ and an integrated total dose of 19 MRad. Three chips were irradiated. Only four SEUs were detected for the shift register corresponding to a cross section of σ = 6.4E-17 cm^2 and σ = 2.2E-17 cm^2 – 1.6E-16 cm^2 at the 95% confidence level. Not a single SEU was detected in the shadow register (only the chip id and counter modulo were tested). This is significantly harder than the SVX3d. The SVX3d SEU cross section obtained in the same beam varied from σ = 2.4E-16 cm^2 to σ = 3.9E-15 cm^2 depending on the proton's incident angle and shift register cell type. No change in the

analog performance was observed: the pedestals, gain, and noise values remained unchanged after the irradiation.

17.2 Total Integrated Doses

The Co-60 gamma ray irradiation occurred at DMEA. A single chip and a 4-chip CDF hybrid were irradiated. Total doses of 16-18 MRad were achieved. The dose rate was 2 MRad/hr. Chips were operated and readout using the LBNL Patt03 DAQ system. Every hour a series of data sets, containing ~1000 events (all channels), were written to disk. Data sets varied in the value of VCAL, bandwidth, applied DVDD and AVDD, and ADC ramp direction. From the data sample, the gain and noise were calculated.
The front end voltages Ncas and Bias were monitored, as well as the preamp input voltage level during reset. After irradiation, the chips were tested again four days later in order to study possible annealing effects.

A single chip sitting on a PCB and a 4-chip CDF hybrid were exposed to the irradiation. They received doses of 17.9 MRad and 15.8 MRad, respectively. Small pedestal shifts and corresponding shifts of the response of channels with charge injection were observed. No obvious change of noise was seen. Finally, a D∅ hybrid was irradiated by 16 MeV protons. The hybrid survived an integrated dose of 25 MRad with no significant change in noise performance.

18 Deadtimeless Operation

Only CDF will be using the deadtimeless operation of the chip. There is a jumper on the SVX4 chip carrier that must be set in order to choose which mode the chip will operate in. It was determined that LBNL would do deadtimeless studies. Chips on the standard chip carrier board and on CDF hybrids were studied.

The general measurement principle is this: first the chip is placed in acquire mode and a L1A is sent at a fixed time at the beginning of the acquire sequence (which happens to correspond to pipeline cell 46). Then chip is placed in digitize and readout mode. The first L1A is needed in order to be able to put the chip in the three different operation cycles. The data thus read out for this L1A is nonsensical and are ignored. In order to check possible pedestal effects related to transitions between the cycles or changes in control signals within the cycles a second L1A is sent. The second L1A is moved bucket by bucket through the above chip's cycles . This is the data we are interested in, thus another digitize and readout sequence follows in order to plot the data as a function of L1A position (or time or front end clocks).

This sequence of chip states (and L1A signals) is repeated. For each bucket, the data marked by the second L1A signal is averaged over. The good news is that there is only one big structure that happens at the end of readout and moves all channels into saturation. There are a number of small structures. So far we identified a pedestal shift when the comparators fire (in the digitize sequence), and another one at the end of readout due to the simultaneous transitions of comp_rst, ramp_rst and rref_sel signals. Also several pipeline errors occur after the big spike at the end of readout.

19 Specifications of the SVX4

We show all the specifications of the SVX4 and the measured values from all combined test stands.

	Design Value	Measured Value
Gain	3 mV/fC	4.4 mV/fC
Gain Uniformity	5% or better	Confirmed
External Load Capacitance	10 pF to 50 pF	Confirmed
Risetime 0-90%	Adjustable in 60-100ns for any load	Confirmed
Risetime Adjustment	4 bits	Confirmed
Noise (ENC)	<2000 e for 40 pF load	2025 e for 69 ns
Linearity	Linear response for pulses up to 20 fC	Confirmed
Dynamic Range	>200 fC	Confirmed
Reset + Settling Time	<1μs for any initial condition	100 ns + 1 FE clk
Calibration Injection	40 fF internal cap	25fF

Table 9 Preamplifier specifications and the measured values.

	Design Value	Measured Value
Voltage Gain	3-5	3.4
Gain Uniformity	5% channel to channel	Confirmed
Risetime 0-90%	10 ns to 40 ns	Confirmed
Noise (ENC)	<500 e	Confirmed
Linearity	Linear response for pulses up to 20 fC	Confirmed
Dynamic Range	>40 fC at preamp input	Confirmed
Reset Time	<20 ns for any allowed condition	25 ns, okay
Pedestal Uniformity	<500 e at preamp input (channel to channel)	Confirmed
	<1000 e at preamp input (cell to cell)	Failed!

Table 10 Pipeline specifications and the measured values.

	Design Value	Measured Value
Ramp Rate Trim Bits	3 bits	Confirmed
Ramp Linearity	0.25% for rates between 0.1 and 1 V/μs	Confirmed
Counter	8 bit Gray code, 106 MHZ rate	Confirmed
Differential Non-Linearity	<0.5 LSB	Confirmed

Table 11 ADC specifications and measured values.

	Design Value	Measured Value
Current Source Range	2.5 mA to 17.5 mA in 2.5 mA steps	Confirmed
Rise and Fall Times	>2ns and < 4ns	Confirmed
Bi-directional	All bus pads are I/O for D∅	Confirmed
Single Ended Use		Confirmed

Table 12 Data Output Driver specifications and measured values.

	Design Value	Measured Value
BN/TN Modes	Only Active in Digitize Mode	Confirmed
Priority In/Out Modes	Configuration register input/output	Confirmed
	Priority passing during Readout Cycle	Confirmed
	Priority Out High during Digitize Cycle	Confirmed

Table 13 Top Neighbor and Bottom Neighbor (TN/BN) specifications and measured values.

	Design Value	Measured Value
Calibration Injection Mask	128 bits	Confirmed
Preamp Bandwidth	3 bits	Confirmed
Ramp Rate	3 bits	Confirmed
Preamp Current	2 bits	Confirmed
Pipeline Write Current	2 bits	Confirmed
Pipeline Read Current	2 bits	Confirmed
Pipeline Depth	6 bits	Confirmed
Driver Current	2 bits	Confirmed
Threshold for Sparsification	8 bits	Confirmed
Counter Modulo	8 bits	Confirmed
Chip ID	7 bits	Confirmed
Dynamical Pedestal Subtraction	1 bit	Confirmed
Read Neighbors	1 bit	Confirmed
Read Channel 63	1 bit	Confirmed
Read Channel 127	1 bit	Confirmed
Pedestal Adjustment	3 bits	Confirmed
Reversed Polarity	1 bit	Confirmed

Table 14 Configuration Register with all functionality.

20 Proposed changes to the SVX4

The have been several proposed changes to the SVX4 that will be implemented in the next version of the chip. We discuss each one of them below.

20.1 Pullup or Pulldown on D∅ mode pad

As stated in the introduction, the chip can be operated in two modes –D∅ and CDF. Presently, the pad that selects this mode, the D∅ mode pad, is floating. That means the pad must be wire bonded to DVDD for the chip to be operated in D∅ mode or it must be wire bonded to GND for the chip to be operated in CDF mode. It has been decided that this pad will be pulled down to GND and that D∅ will have to wire bond it to AVDD to place the chip is D∅ mode. Suppose that the wire bond connecting this pad to the hybrid fails, the chip will go into the default mode (CDF).

20.2 Pullup on USESEU pad

As stated in the introduction, the current version of the chip allows the user to decide which register to initialize the chip from. If the USESEU pad is wire bonded to ground, the operating parameters will be taken from the shift register. If the USESEU pad is wire bonded to DVDD, the operating parameters will be taken from the SEU register (or shadow register). Since the SEU register design has been confirmed to work and is radiation hard, this will be the default configuration. As a side note, the shift register cannot be used due to the Catch-22 effect of the driver currents changing as the initialization bit stream is downloaded. For example, if a new bit stream is downloaded, the bit field corresponding to the output drivers changes and affects the chip readout.

20.3 Pullup of Bit 7 on Chip ID

The chip ID only goes up to 128, so that leaves one extra bit in the 8 bit readout bus that is arbitrary. Since the SVX4 will be operating in sparse mode in the experiment, it becomes possible to misinterpret the chip ID as a channel number followed by its data because the length of the readout is unknown. By pulling up bit 7 of the chip ID output, the channel IDs are effectively changed to 129-255. Therefore it becomes impossible to misinterpret the chip ID with a channel number. Note: there are 128 channels that can have data values from 0-255.   The channel numbers are hardwired in the readout. In Figure 42, we show the output of the chip id scan from the Stimulus System.
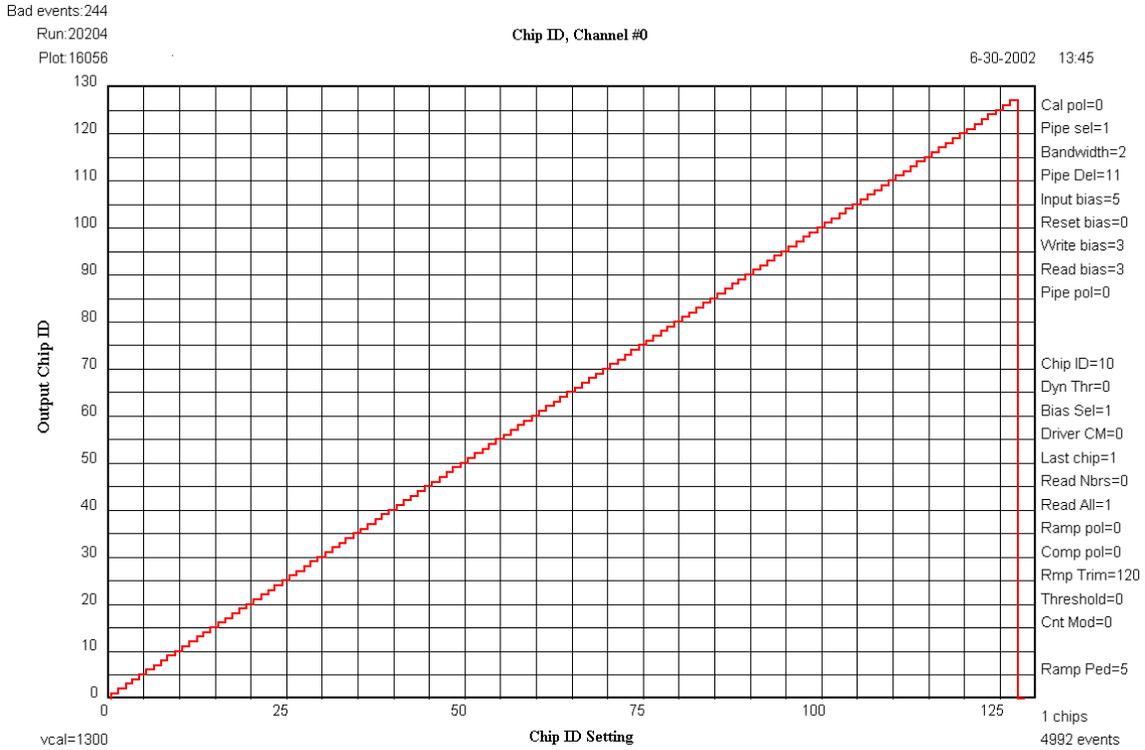
Figure 42 Histogram showing a chip ID scan. The x-axis shows the value of the chip ID that was downloaded to the chip and the y-axis shows that value of the chip ID that was read from the chip in readout cycle.

20.4 Pull down of Bit 6 and Bit 7 on Cell ID

Since there are only 47 pipeline cells that can be used, the status word does not need all 8 bits similar to the chip ID. It is easier to read out the pipeline cell number directly into the DAQ system if the upper two non-used bits are pulled down or always zero.

20.5 Hardwiring PRIOUT driver strength bits

During early testing of the SVX4, it was noticed that when the SVX4 is initialized using the shift register as opposed to the USESEU register, the parameters were not downloaded correctly. This is because the downloaded bit stream was changing the bits of the PriOut driver and therefore the output was skewed.

20.6 Adding two more bits to the shift register

The current length of the download of the SVX4 is 190 bits. This does not fall with a word boundary, or said another way, 190 is not divisible by eight. Adding an additional two bits makes the downloading length fit within a word boundary. These additional bits can also be used for additional functionality if needed. One such use is described below.

20.7 Changing latching scheme for ADC control in D∅ mode

There is a design flaw in the SVX4 that was not realized in the simulation. The design flaw is that the front end clock is not gated during the digitization in D∅ mode. This makes it impossible in D∅ mode to place the pipeline cell onto the write amplifier. There is a work around that is complicated and will affect the rate and deadtime of the chip when operating in D∅ mode by modifying the control pattern sent to the chip. The modification inside the chip is to gate the front clock in every cycle of the chip except readout. This modification will make the digitization process easier and will decrease the amount of deadtime of the chip, but the control lines must have there proper values in all cycles of the chip.

20.8 Adding a V cal switch

Because the D∅ hybrids or D∅ purple card cannot source enough current to set the V cal voltage properly, it has become attractive to have a switch that will turn off the V cal voltage and allow an external pulser to be used to calibrate the system. The extra two bits that would be added as discussed above allow one bit to have the functionality to turn off V cal and the other bit to be a dummy.

20.9 Adding on-chip decoupling capacitors to BIAS

The use of on chip bypassing for the power AVDD has led to the proposal of the idea to bypass the BIAS with on chip bypassing as well. There is enough space on the chip to do this. This removes one extra component from the hybrid that will be needed.

20.10 Layout and Design changes to the ADC comparator and improvements.

There have been many suggestions to improve the performance of the ADC. The biasing scheme of the comparators will be modified in order to improve the response time of the comparators. Currently, the pedestal can only be lowered to 60 ADC counts due to the analog delay in the chip. The analog delay in the circuit is there to produce an observable baseline with DPS on so noise studies could be done. The submission of two versions in the next production run will be discussed below.

20.11 Modifying the LVDS receiver

It has been found that lowering or raising the I quiescent current will prevent the receiver from working properly. This is because there is a size mismatch in the p and n FETs that make up the receiver. Increasing the size of the p FETs of the receivers will correct this problem and the chip will work properly for large values of I quiescent. There is also a discussion to remove the receiver from I quiescent and bias it through an independent transistor.

20.12 Increasing the width of the Pipeline Metal

As discussed above, there is a nonuniformity in the pipeline which is currently not understood. It is believed to be coming from resistance in the traces that go to the

capacitors in the pipeline which slightly alters the gain for each individual channel of the pipeline.

20.13 NMOS Guard Rings

It was found that the NMOS transistors in the chip do not have a PMOS guard ring included, which is standard practice for making radiation hard electronic circuitry. The new submission of the chip will contain the PMOS guard rings around all NMOS transistors.

21 Traps and Pitfalls

Usually, the acquired knowledge and experience from chip testing is passed down by word of mouth. This section is an attempt to document the experience gained while testing the prototype SVX4 chips. This section may lack coherence and fluidity, but that is a small price to pay in order to have a list of the nuances learned from early testing.

21.1 Pipeline Cell 63

It was found during testing that pipeline 63 was being returned from the chip while testing. There were a variety of reasons that this occurred. First, it the mode lines are not properly set to enter the acquire cycle, it appeared that the pipeline logic simply defaulted to pipeline 63. Second, this could also occur if no Level 1 accept was received by the chip while in the acquire cycle.

21.2 L1A in conjunction PRD2

It was found during testing by the designers that in deadtimeless mode, if the Level 1 accept was received while the PRD2 was being issued, the chip sometimes would not see the Level 1 accept. This is because there are strict time constraints that must be adhered to during this cycle of operation. The PRD2 pulse must be wide enough so there is no conflict between the rising and falling edges of the pulses.

21.3 Incomplete readout or zeros in the data

It was also found that sometimes the data read back from the chip while in read all mode did not read back all the channels or that the data contained a majority of zeros. Sometimes the data read back was incomplete.

It was found that it was necessary to be completely sure about the number of clock edges that the chip received in digitization mode. Sending 256 edges is not enough to complete the digitization process. It is necessary to send two extra clock pulses in order to synchronize the output latch with the clock. If these two clock pulses were not sent it was possible that the data value from the channel would not be latched in.

Also, a timing violation in the readout FIFOs occurs in the chip if the ramp and comparator reset setting were not maintained at the proper digital level during the complete digitization cycle. It was found that either the readout was incomplete or readout would fail completely. Once the comparator reset and ramp reset are released, they must remain in that condition until the readout cycle commences.

22 The Future

It has been decided to take two approaches for the next submission of the SVX4. We are going to submit two different designs: minimal changes and maximal changes. The minimal change plan will literally make minimal changes that will correct the pedestal nonlinearity therefore making it low risk because we presently have a working chip. The minimal changes included increasing the internal bias current of the comparators to decrease the nonlinearity and channel to channel variation in the comparators as well as including PMOS guard rings around all the NMOS transistors inside the chip. This version will be called version A.

The maximal changes model incorporates redesigning of the ADC, but keeping the same architecture. The ramp will be redesigned as well as the ramp pedestal generator. The front end metal inside the pipeline will be increased in an attempt to decrease the nonuniformity of the pipeline. This version will be called version B.
The retical will be divided into a 5:1 ratio, with 5 version Bs and 1 version A. It has been decided that if the redesigned ADC does not work that we will have enough version As from the submission and a working mask for further submissions of the chip.

23 Conclusions

We have extensively tested the SVX4 chip using the Stimulus Test Stand. We have confirmed the specifications that have been specified and have documented the specifications that have not been satisfied.

The three critical issues are pedestal nonuniformity, channel to channel variations, and pipeline nonuniformity. Each issue has been addressed and discussed in this paper. The biasing of the comparators is the reason for the pedestal nonuniformity and the channel to channel variation. No solid explanation has been found for the pipeline uniformity.
The next submission of the chip will have two versions. Version A is a fall back version with minimal changes in order to insure both experiments will have a working version of the chip to test. Version B is a more aggressive version with a newly redesigned ADC and ramp generator.

24 Acknowledgements

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[1] L. Christofek et al., D∅ Note 4252.

[2] L. Christofek et al., D∅ Note 4250.

[3] K. Hanagaki, M. Garcia-Sciveres, and M. Weber, D∅ Note 4015.

[4] This time is dependent on the front end clock frequency and duty cycle. Two other factors must be taken into account when calculating the gain: 1) the frequency of digitization and 2) the slope of the ramp. Increasing the digitization frequency decreases the gain. Similarly, increasing the slope of the ramp decreases the gain.

[5] We discuss the pedestal nonuniformity in Section 16.1.

[6] Martin Rehn et al., Statistical Study of SVX3D Chip Dynamic Pedestal Subtraction Threshold Level.

[7] Variations of the baseline with DPS on give a first-order measurement of the noise.

[8] The Stimulus System DAQ is limited to 50 MHz because the FIFOs on the Adaptor Board are limited by that clocking speed or ability to clock in data.

[9] A data cycle consisted of 240 single events.

[10] T. Bolton, K. Carnes, T. Gray, A. Rankin, E. von Toerne, D∅ Note 4149.